Configurable H-Bridge Driver

FEATURES

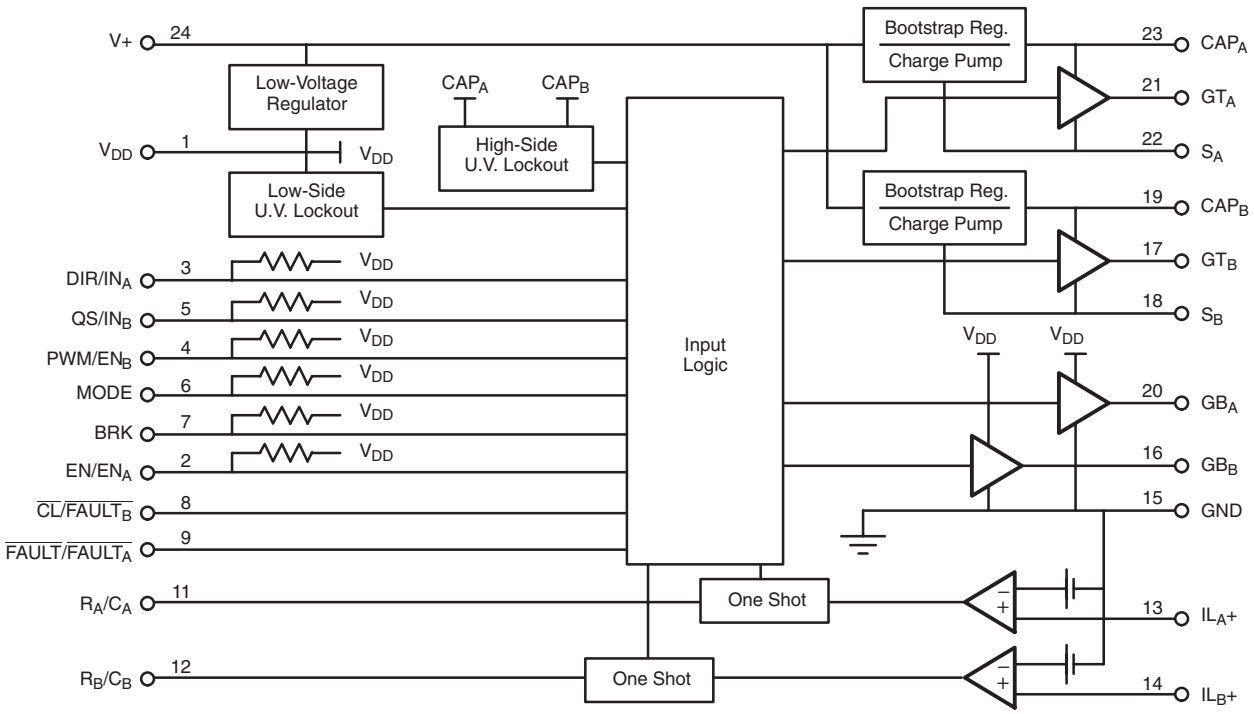
- H-Bridge or Dual Half-Bridge Operation
- 20- to 40-V Supply
- Static (dc) Operation
- Cross-Conduction Protected
- Current Limit
- Undervoltage Lockout
- ESD Protected
- Fault Output

DESCRIPTION

The Si9978 is an integrated driver for an n-channel MOSFET H-bridge. The mode control allows operation as either a full H-bridge driver or as two independent half-bridges. The DIR/PWM input configuration allows easy implementation of either sign/magnitude or anti-phase PWM drive schemes for full H-bridges. Schmitt triggers on the inputs provide logic signal compatibility and hysteresis for increased noise immunity. An internal low-voltage regulator allows the device to be powered directly from a system supply of 20 to 40 volts. All n-channel gates are driven directly from low-impedance outputs. The addition of one external capacitor per half-bridge allows internal circuitry to level shift both the power supply and logic signal for the high-side n-channel gate drives. Internal charge pumps replace leakage current lost in the high-side driver circuits to provide “static” (dc) operation in any output condition. Protection features include an undervoltage lockout, cross-conduction prevention logic, and overcurrent monitors.

The Si9978 is available in both standard and lead (Pb)-free, 24-pin wide-body SOIC (surface mount) packages, specified to operate over the industrial (–40 to +85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on pins 2–7 with respect to ground . . . . . –0.3 to V_{DD} + 0.3 V
Voltage on pin 24 . . . . . –0.3 to 50 V
Voltage on pins 17, 19, 21, 23 . . . . . –0.3 to +60 V
Voltage on pins 18, 22 . . . . . –2 to 50 V

Operating Temperature (T_A) . . . . . –40 to +85°C
Storage Temperature . . . . . –65 to 150°C
Maximum Junction Temperature (T_J) . . . . . 150°C
Power Dissipation . . . . . 500 mW

RECOMMENDED OPERATING CONDITIONS

V+ . . . . . +20 to 40 V_{DC}
R_A, R_B . . . . . 100 kΩ

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 20 to 40 V	Limits –40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Power						
Supply Voltage Range	V+		20		40	V
Logic Voltage	V_{DD}		14.5	16	17.5	
Supply Current	I+	I_{DD} = 0 mA		3	5	mA
Inputs (DIR, PWM, EN, QS, MODE, BRK)						
High-State	V_{IH}		4.0			V
Low-State	V_{IL}				1.0	
High-State Input Current	I_{IH}	$V_{IH} = V_{DD}$			10	µA
Low-State Input Current	I_{IL}	V_{IL} = 0 V	–100	–50	–25	
Outputs						
Low-Side Gate Drive, High State	V_{GBH}		14	16	17.5	V
Low-Side Gate Drive, Low State	V_{GBL}				1	
High-Side Gate Drive, High State	V_{GTH}	$S_{A, B}$ = 0 V	14	16	18	
High-Side Gate Drive, Low State	V_{GTL}				1	
Low-Side Switching, Rise Time	t_{rL}	Rise Time = 1 to 10 V Fall Time = 10 to 1 V C_L = 600 pF		110		ns
Low-Side Switching, Fall Time	t_{fL}			50		
High-Side Switching, Rise Time	t_{rH}			110		
High-Side Switching, Fall Time	t_{fH}			50		
Break-Before-Make Time				250		
$\overline{FAULT}$, $\overline{CL}$	V_{OL}	I_{OL} = 1 mA			0.4	V
$\overline{FAULT}$, $\overline{CL}$ Leakage Current	I_{OH}	$\overline{FAULT}$, $\overline{CL}$ = V_{DD}		0.2	10	µA
Protection						
Low-Side Undervoltage Lockout	UVLL			0.8 V_{DD}		V
Low-Side Hysteresis	V_H			0.8		
High-Side Undervoltage Lockout	UVLH	$S_{A, B}$ = 0 V		V_{DD}–3.3 V		
Current Limit						
Comparator Input Bias Current	I_{IB}		–5	–0.2	5	µA
Comparator Threshold Voltage	V_{TH}	T_A = 25°C	90	100	110	mV
			85		115	
One Shot Pulse Width	t_p	R_A, R_B = 100 kΩ, C_A, C_B = 100 pF	8	10	12	µs
		R_A, R_B = 100 kΩ, C_A, C_B = 0.001 µF	80	100	120	
Propagation Delay	t_{pd}	C_L = 600 pF		600		ns

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

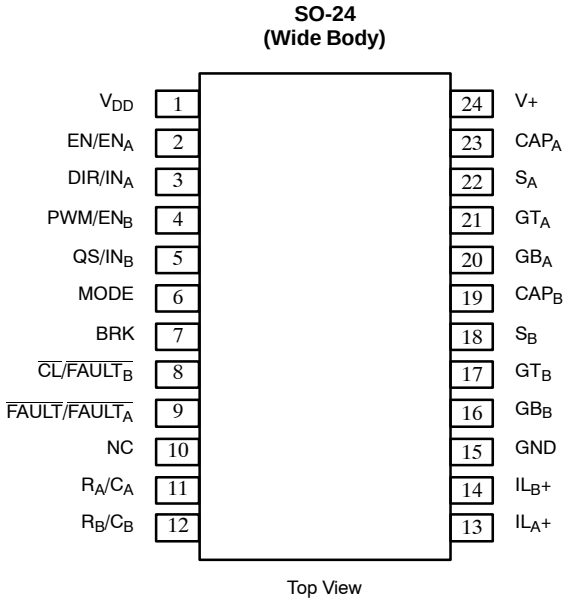
TRUTH TABLE—H-BRIDGE MODE

MODE	DIR/ IN_A	EN/ EN_A	QS/ IN_B	PWM/ EN_B	BRK	IL_A+	IL_B+	GT_A	GB_A	GT_B	GB_B	$\overline{CL}$/ $\overline{FAULT_B}$	FAULT/ $FAULT_A$	Condition
1	1	1	1	⎍	0	L	X	H	L	L	⎍	1	1	Normal Operation
1	1	1	0	⎍	0	L	X	⎍	L	L	⎍	1	1	
1	0	1	1	⎍	0	L	X	L	⎍	H	L	1	1	
1	0	1	0	⎍	0	L	X	L	⎍	⎍	L	1	1	
1	X	1	X	X	1	L	X	L	H	L	H	1	1	Brake
1	X	0	X	X	X	L	X	L	L	L	L	1	1	Disable
1	X	1	X	X	0	⎍	X	L	L	L	L	⎍	⎍	Overcurrent
1	X	X	X	X	X	X	X	L	L	L	L	1	0	Undervoltage on V_{DD}

TRUTH TABLE—HALF-BRIDGE MODE

MODE	DIR/ IN_A	EN/ EN_A	QS/ IN_B	PWM/ EN_B	BRK	IL_A+	IL_B+	GT_A	GB_A	GT_B	GB_B	$\overline{CL}$/ $\overline{FAULT_B}$	FAULT/ $FAULT_A$	Condition
0	1	1	X	0	X	L	L	H	L	L	L	1	1	Normal Operation
0	0	1	X	0	X	L	L	L	H	L	L	1	1	
0	X	0	1	1	X	L	L	L	L	H	L	1	1	
0	X	0	0	1	X	L	L	L	L	L	H	1	1	
0	X	1	X	X	X	⎍	X	L	L	X	X	1	⎍	Overcurrent on A
0	X	X	X	1	X	X	⎍	X	X	L	L	⎍	1	Overcurrent on B
0	X	X	X	X	X	X	X	L	L	L	L	0	0	Undervoltage on V_{DD}

PIN CONFIGURATION AND ORDERING INFORMATION



ORDERING INFORMATION			
Part Number	Lead (Pb)-Free Part Number	Temperature Range	Package
Si9978DW		–40 to 85°C	SOIC-24 (Wide Body)
Si9978DW-T1	Si9978DW-T1—E3		

PIN DESCRIPTION

Pin 1: V_{DD}

V_{DD} is an internally generated voltage. It is connected to this pin to allow connection of a decoupling capacitor. A minimum of 1 μF is recommended.

Pin 2: EN/EN_A

The EN input allows normal operation when at logic “1”, and turns all gate drive outputs off when at logic “0”. When the mode pin is at logic “1”, EN controls the entire H-bridge. When the mode pin is at logic “0”, this pin becomes the ENABLE pin for half-bridge A.

Pin 3: DIR/IN_A

The function of this pin is determined by the MODE pin. When the MODE pin is at logic “1”, it is the DIR pin, and when MODE is at logic “0”, it is the IN_A pin.

As the DIR input, it is the direction control for the H-bridge, and determines which diagonal pair of power MOSFETs is active. A logic “1” turns on GT_A and enables GB_B, while a logic “0” turns on GT_B and enables GB_A. When implementing an anti-phase PWM control, the DIR input serves as the PWM input.

As the IN_A pin, it is the input that controls the “A” half-bridge. When at logic “1”, the high-side MOSFET is turned on, and when at logic “0”, the low-side MOSFET is turned on.

Pin 4: PWM/EN_B

With the mode pin at logic “1”, this pin is the PWM input. It controls the switching of the active diagonal pair. A logic “1” turns the active MOSFETs on, while a logic “0” turns it off. The QS input determines whether the bottom or both bottom and top MOSFETs are switched. When implementing an anti-phase PWM control, the PWM input is connected to a logic “1”. When the mode pin is at logic “0”, this pin becomes the ENABLE pin for half-bridge B.

Pin 5: QS/IN_B

With the mode pin at logic “1”, this input determines whether the bottom MOSFETs of the H-bridge or both bottom and top MOSFETs switch in response to the PWM signal. A logic “1” on this input enables only the bottom MOSFETs. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, both the bottom and top MOSFETs are enabled.

This input controls the B half-bridge when the MODE pin is at logic “0”. When at logic “1”, the high-side MOSFET is turned on, and when at logic “0”, the low-side MOSFET is turned on.

PIN DESCRIPTION (CONT'D)

Pin 6: MODE

This input determines whether the Si9978 functions as an H-bridge or as two independent half-bridges. When the MODE pin is at logic "1", the Si9978 functions as an H-bridge, and when MODE is at logic "0", it functions as two independent half-bridges.

Pin 7: BRK

When this input and MODE are at logic "1", both bottom gate drives are switched high, turning on the bottom MOSFETs. When this input is at logic "0", the Si9978 operates normally.

Pin 8: $\overline{CL}/\overline{FAULT_B}$

This is an open drain output which is active low. When the MODE pin is at logic "1", this pin functions as $\overline{CL}$ and indicates that the H-bridge is in current limit. It stays low for the duration of the current limit one-shot. With the MODE pin at logic "0", it serves as the $\overline{FAULT}$ output for half-bridge B to indicate when an undervoltage or overcurrent condition is detected. When indicating an overcurrent condition, the output stays low for the duration of the current limit one-shot. The $\overline{FAULT}$ output resets automatically when the condition clears.

Pin 9: $\overline{FAULT}/\overline{FAULT_A}$

This is an open drain output which is switched low when an undervoltage or overcurrent condition is detected. When indicating an overcurrent condition, the output stays low for the duration of the current limit one-shot. When the MODE pin is at logic "1", this pin is the H-bridge $\overline{FAULT}$ output. With the MODE pin at logic "0", it serves as the $\overline{FAULT}$ output for half-bridge A. The $\overline{FAULT}$ output resets automatically when the condition clears.

Pin 10: NC

No internal connection.

Pin 11: R_A/C_A

The timing resistor and capacitor for the current limit one-shot are connected to this pin. The values of the resistor and capacitor determine the off time set by the one-shot. The one-shot is triggered when the current limit comparator detects an overcurrent condition.

Pin 12: R_B/C_B

The timing resistor and capacitor for the current limit one-shot are connected to this pin. The values of the resistor and capacitor determine the off time set by the one-shot. The one-shot is triggered when the current limit comparator detects an overcurrent condition.

Pin 13: IL_A+ and Pin 14, IL_B+

These are the overcurrent sense inputs. Internally, they are connected to the noninverting inputs of the current limit comparators. Externally they are connected to the source(s) of the low-side MOSFET(s) and the current sense resistor.

Pin 15: GND

The GND pin is the ground return for V+ and the ground reference for the logic. Also, this is the ground reference input for the current limit comparators and is connected to the ground side of the internal 100-mV references. This pin should be connected directly to the ground side of the current sensing resistors.

Pin 16: GB_B and Pin 20, GB_A

These pins drive the gates of the low-side power MOSFETs.

Pin 17: GT_B and Pin 21, GT_A

These pins drive the gates of the high-side power MOSFETs.

Pin 18: S_B and Pin 22, S_A

These are the source connections of the high-side power MOSFETs, the drain of the external low-side power MOSFET, the negative terminal of the bootstrap capacitor, and the output for each half-bridge.

Pin 19: CAP_B and Pin 23, CAP_A

These are the connections for the positive terminals of the bootstrap capacitors C_{BA} and C_{BB}. A 0.01-μF capacitor can be used for most applications.

Pin 24: V+

This is the only external power supply required for the Si9978, and must be the same supply used to power the H-bridge it is driving. The Si9978 powers the low-voltage logic, low-side gate driver, and bootstrap/ charge pump circuits from self-contained voltage regulators which require only a bootstrap capacitor on the CAP pins.

No voltage sensing circuitry monitors V+ directly; however, the low-voltage, internally generated supply and the bootstrap voltage (which are derived from V+) are directly protected by undervoltage monitors.

APPLICATION CIRCUIT

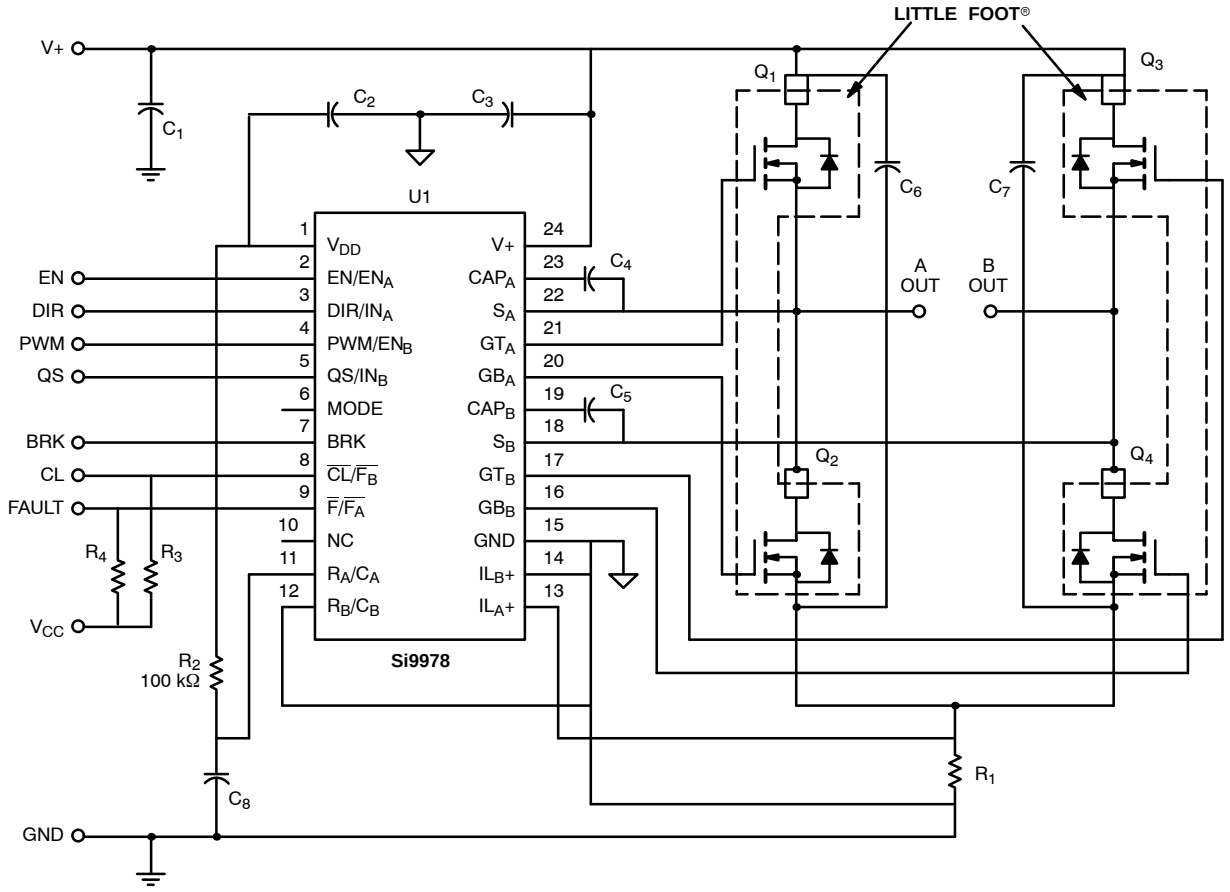
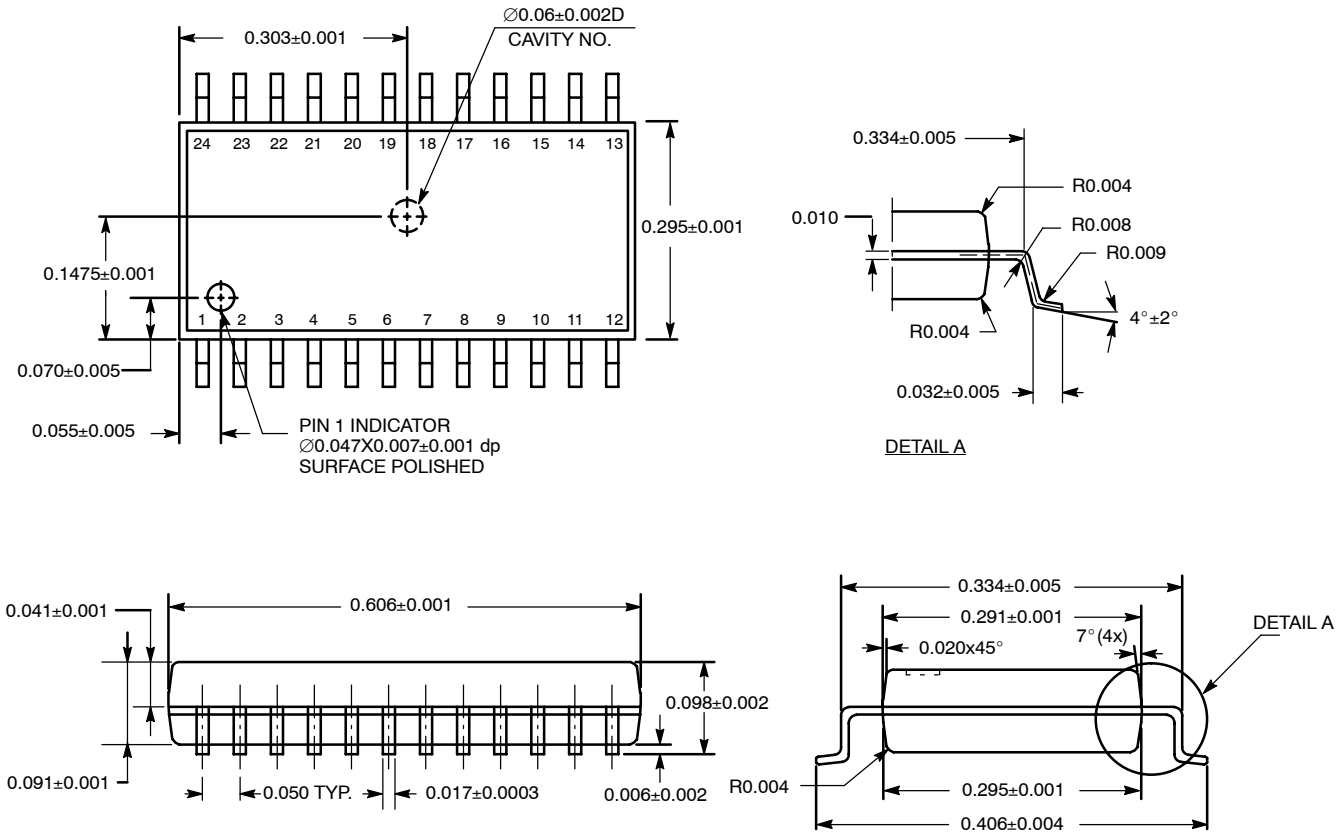


FIGURE 1. Basic H-Bridge Circuit

SOIC (WIDE-BODY): 24-LEAD (POWER IC ONLY)



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