# SRK2001

Datasheet

## Adaptive synchronous rectification controller for LLC resonant converter


**Product status link**

SRK2001

**Product label**

SUSTAINABLE TECHNOLOGY

## Features

- Secondary side synchronous rectification controller optimized for LLC resonant converter
- Dual gate driver for N-channel MOSFET
- Adaptive turn-off logic
- Turn-on logic with adaptive masking time
- Auto-compensation of parasitic inductance
- Low consumption mode: 50 µA quiescent current
- $V_{CC}$ operating voltage range 4.5 V to 32 V
- High voltage drain-to-source Kelvin sensing for each SR MOSFET
- 35 ns total delay at turn-off
- Protection against current reversal
- Safe management of load transient, light-load and startup conditions
- Intelligent automatic sleep mode at light-load with user programmable enter/exit load levels, with soft transitions and function disable
- Programmable exit load levels from burst mode
- Compatible with standard level MOSFET
- SSOP10 package

## Applications

- AC-DC adapters
- All-in-one PC
- High-end flat panel TV
- 80+/85+ compliant ATX SMPS
- 90+/92+ compliant SERVER SMPS
- Industrial SMPS

## Description

The SRK2001 controller implements a control scheme specific for secondary side synchronous rectification in LLC resonant converters that use a transformer with center tap secondary winding for full wave rectification.

It provides two high current gate drive outputs, each capable of directly driving one or more N-channel power MOSFET. Each gate driver is controlled separately and an interlock logic circuit prevents the two synchronous rectifier MOSFET from conducting simultaneously.

The control scheme ensures that each synchronous rectifier is switched ON as the corresponding half-winding starts conducting and OFF as its current falls to zero.

The turn-on logic with adaptive masking time and adaptive turn-off logic allow maximizing the conduction time of the SR MOSFET, eliminating the need for a parasitic inductance compensation circuit.

The low consumption mode of the device allows meeting the most stringent requirements for converter power consumption in light-load and no-load conditions.

A very low external component count is required when using this device.

# 1 Block diagrams

Figure 1. **Internal block diagram**

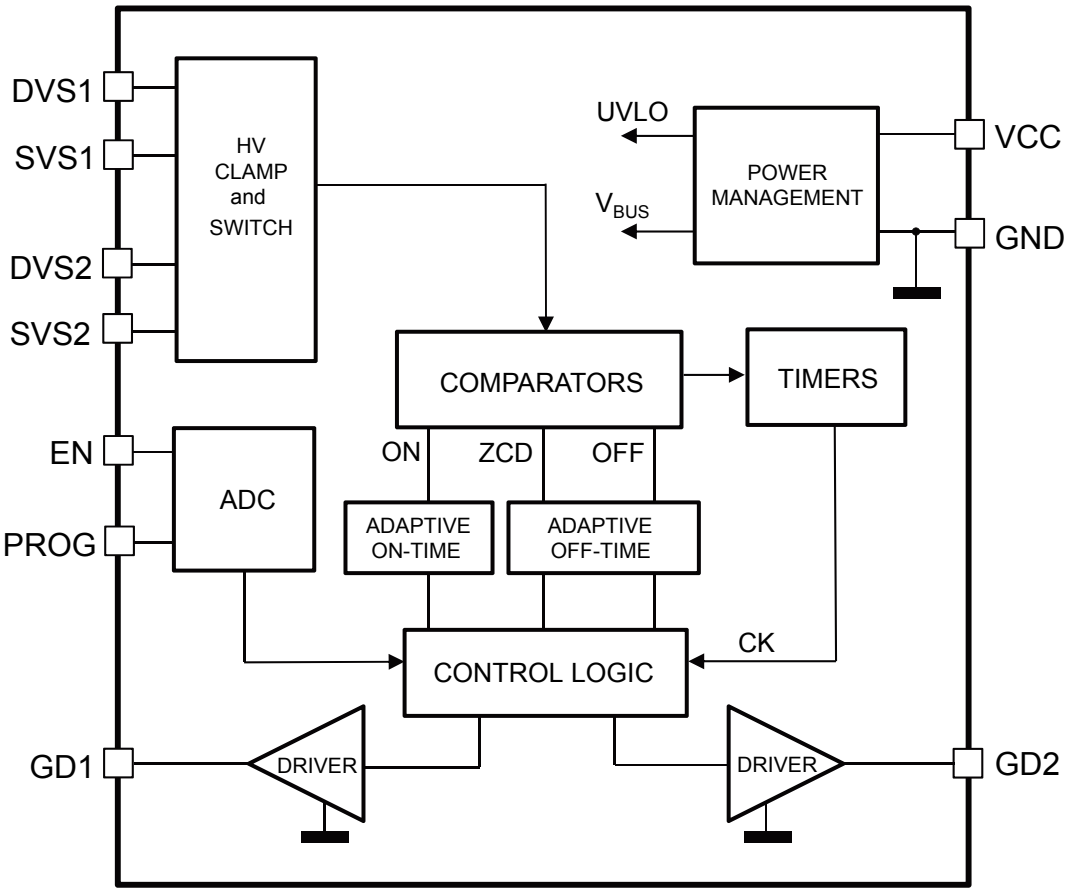
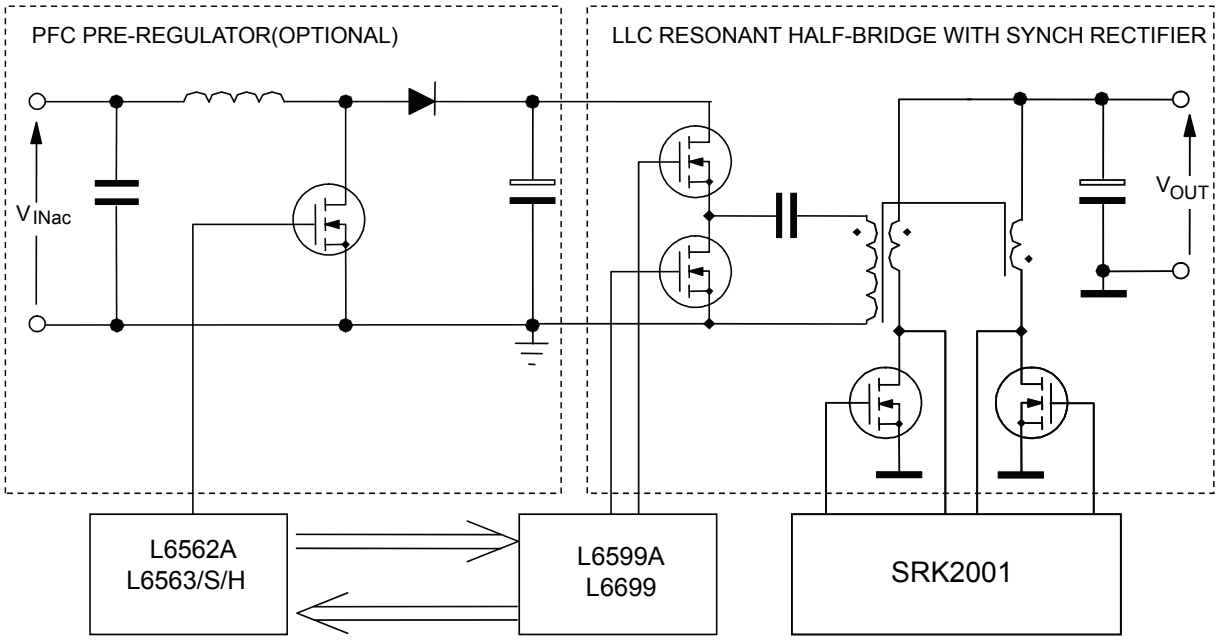



Figure 2. **Typical system block diagram**



## 2 Pin connections and functions

Figure 3. **Pin connections (top view)**

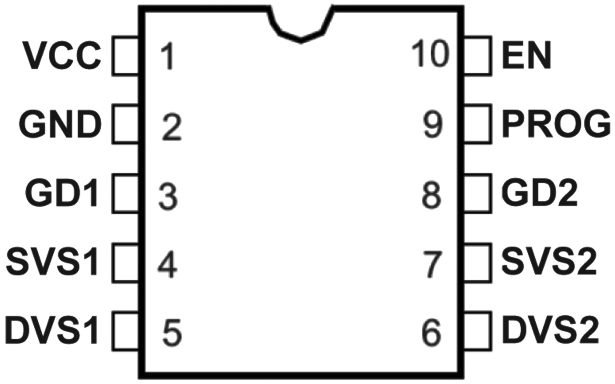



Table 1. **Pin functions**

| No. | Name | Function |
|---|---|---|
| 1 | VCC | Supply voltage of the device. A bypass capacitor to GND located as close to IC pins as possible helps to obtain a clean supply voltage for the internal control circuitry and acts as an effective energy buffer for the pulsed gate drive currents. |
| 2 | GND | Return of the device bias current and return of the gate drive currents. Route this pin to the common point where the source terminals of both synchronous rectifier MOSFET are connected. |
| 3 (8) | GD1 (GD2) | Gate driver output for section 1 (2). Each totem pole output stage is able to drive power MOSFET with high peak current levels. To avoid excessive gate voltages when the device is supplied with a high $V_{CC}$, the high-level voltage of these pins is clamped to about 11 V. The pin has to be connected directly to the SR MOSFET gate terminal. |
| 4 (7) | SVS1 (SVS2) | Source voltage sensing for section 1 (2): it is the reference voltage of the corresponding drain sensing signal on the DVS1,2 pin. These pins have to be connected directly to the respective source terminals of the corresponding synchronous rectifier MOSFET. |
| 5 (6) | DVS1 (DVS2) | Drain voltage sensing for section 1 (2). These pins have to be connected to the respective drain terminals of the corresponding synchronous rectifier MOSFET using a series resistor of 100 Ω. |
| 9 | PROG | Programming pin for conduction duty cycle on sleep mode entry/exit. A resistor connected from this pin to GND, supplied by an internal precise current source, sets a voltage $V_{PROG}$; depending on this voltage level, during the startup phase, the user can chose, according to the application requirements, the proper sleep mode or burst mode exiting the conduction duty cycle among the ones contained into two internal lookup tables (the values are predefined inside Table 5, Table 6 and Table 7). SeeTable 4 for the proper choice of resistor value. |
| 10 | EN | Enable pin function with internal pull-up and current source capability:<br>– Automatic sleep mode function enable/disable: the sleep mode is disabled if the pin voltage is detected above an internal threshold ($V_{SM\_off}$) during the startup phase.<br>– Remote ON/OFF: during run the mode, when the pin voltage is sensed below the internal threshold $V_{EN\_OFF}$, the controller stops operating and enters a low consumption state; it resumes operation if the pin voltage exceeds the threshold $V_{EN\_ON}$.<br>– During the startup phase, the pin voltage level allows selection of the predefined conduction duty cycle for sleep mode entering. A resistor connected from this pin to GND, supplied by an internal precise current source allows the user for this choice (two predefined values). See Table 4 to find the appropriate resistor value. |

# 3 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Pin | Parameter | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | 1 | DC supply voltage | -0.3 to $V_{CCZ}$ | V |
| $I_{CCZ}$ | 1 | Internal Zener maximum current ($V_{CC}$ = $V_{CCZ}$) | 25 | mA |
| $V_{PROG}$ | 10 | PROG pin voltage rating | -0.3 to 3.3 | V |
| $V_{EN}$ | 9 | EN pin voltage rating | -0.3 to 3.3 | V |
| DVS1,2 | 5, 6 | Drain sense voltage referred to source SVS1,2 | -3 to 90 | V |
| SVS1,2 | 4, 7 | Source sense voltage referred to GND | -3 to 3 | V |

Stressing the device above the rating listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum rated conditions may affect device reliability.

# 4 Thermal data

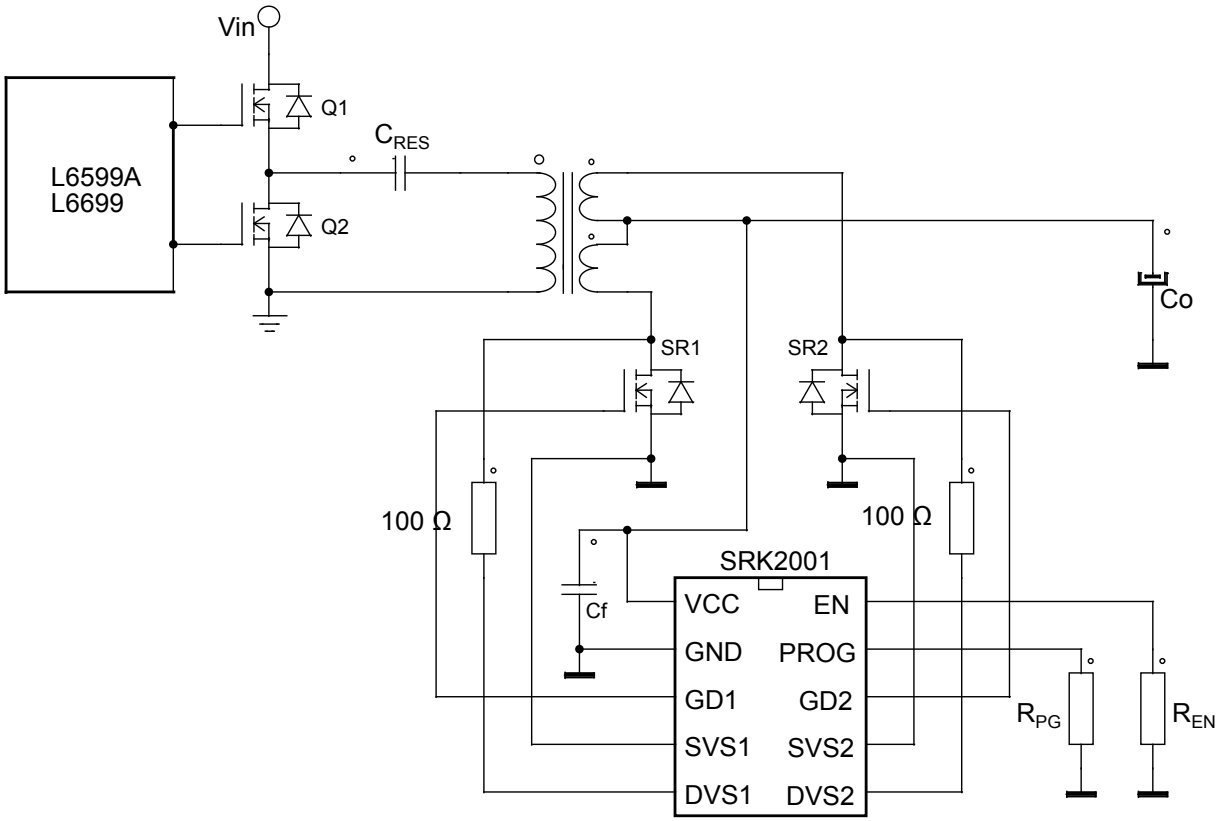
**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Max. thermal resistance, junction to ambient(1) | 130 | °C/W |
| $R_{th\ j\text{-}case}$ | Max. thermal resistance, junction to case top(1) | 10 | °C/W |
| $P_{tot}$ | Power dissipation at $T_{amb}$ = 50 °C | 0.75 | W |
| $T_j$ | Junction temperature operating range | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

1. *With the pin 2 soldered to a dissipating copper area of 25 mm2, 35 µm thickness (PCB material FR4 1.6 mm thickness).*

# 5 Typical application schematic

Figure 4. **Typical application schematic**



# 6 Electrical characteristics

**Table 4. Electrical characteristics**

($T_j$ = -25 to 125 °C, $V_{CC}$ = 12 V, $C_{GD1}$ = $C_{GD2}$ = 4.7 nF, $R_{PG}$ = 0 Ω; unless otherwise specified, typical values refer to $T_j$ = 25 °C).

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply section** | | | | | | |
| $V_{CC}$ | Operating range | After turn-on | 4.5 | - | 32 | V |
| $V_{CC\_On}$ | Turn-on supply voltage | (1) | 4.25 | 4.5 | 4.75 | V |
| $V_{CC\_Off}$ | Turn-off supply voltage | (1) | 4 | 4.25 | 4.5 | V |
| Hys | Hysteresis | - | - | 0.25 | - | V |
| $V_{CCZ}$ | Clamp voltage | $I_{CCZ}$ = 20 mA | 33 | 36 | 39 | V |
| $I_{q\_run}$ | Current consumption in run mode | After turn-on (excluding SR MOS gate capacitance charging/ discharging) at 100 kHz | - | 700 | - | µA |
| $I_{CC}$ | Operating supply current | At 300 kHz | - | 35 | - | mA |
| $I_q$ | Quiescent current | Low-consumption mode operation, with DVS1,2 pins not switching(2), $T_j$ = -25 °C to 85 °C | - | 50 | 65 | µA |
| **Drain-source sensing inputs and synch functions** | | | | | | |
| $V_{DS1,2\_H}$ | Drain-to-source sensing operating voltage | - | - | - | 90 | V |
| $V_{TH\_A}$ | Arming voltage | Positive-going edge | - | 1.4 | - | V |
| $V_{TH\_PT}$ | Pre-triggering voltage | Negative-going edge | - | 0.7 | - | V |
| $V_{TH\_ON}$ | Turn-on threshold | Negative-going edge | -130 | -100 | -70 | mV |
| $T_{diode\_off}$ | Body diode residual conduction time after turn-off | - | - | 75 | - | ns |
| $T_{D\_On\_min}$ | Minimum turn-on delay | - | - | 100 | - | ns |
| $T_{D\_On\_max}$ | Maximum turn-on delay | At 100 kHz | - | 2 | - | µs |
| **Enable pin remote on/off function** | | | | | | |
| $V_{EN\_OFF}$ | Disable threshold | (1)Negative-going edge during run mode | 0.25 | 0.3 | 0.35 | V |
| $V_{EN\_ON}$ | Enable threshold | (1)Positive-going edge during run mode | 0.45 | 0.62 | 0.82 | V |
| $I_{EN\_run}$ | Sourced current | During run mode | 4 | 6 | 8 | µA |
| **Automatic sleep mode programming** | | | | | | |
| $D_{OFF}$ | Min. operating duty cycle to enter sleep mode | $R_{EN}$ = 100 k Ω 1% | - | 40 | - | % |
| | | $R_{EN}$ = 180 k Ω 1% | - | 25 | - | |
| $D_{ON}$ | Restart duty cycle from sleep mode with $R_{EN}$ = 100 kΩ 1% | $R_{PG}$ = 0 Ω | - | 80 | - | % |
| | | $R_{PG}$ = 100 kΩ 1% | - | 75 | - | |
| | | $R_{PG}$ = 180 kΩ 1% | - | 65 | - | |
| | | $R_{PG}$ open | - | 60 | - | |
| $D_{ON}$ | Restart duty cycle from sleep mode with $R_{EN}$ = 180 kΩ 1% | $R_{PG}$ = 0 Ω | - | 75 | - | % |
| | | $R_{PG}$ = 100 kΩ 1% | - | 70 | - | |
| | | $R_{PG}$ = 180 kΩ 1% | - | 60 | - | |

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $D_{ON}$ | Restart duty cycle from sleep mode with $R_{EN}$ = 180 kΩ 1% | $R_{PG}$ open | - | 55 | - | % |
| **Burst-mode exiting programming** | | | | | | |
| $D_{ON\_BM}$ | Restart duty cycle with EN pin open at startup during primary burst mode operation | $R_{PG}$ = 0 Ω | - | 80 | - | % |
| | | $R_{PG}$ = 100 kΩ 1% | - | 75 | - | |
| | | $R_{PG}$ = 180 kΩ 1% | - | 65 | - | |
| | | $R_{PG}$ open | - | 0 | - | |
| $I_{PROG}$ | Sourced current | (1)At $V_{CC}$ startup | 9 | 10 | 11 | µA |
| **Gate drivers** | | | | | | |
| $I_{source\_pk}$ | Output source peak current | (3) | - | -0.35 | - | A |
| $I_{sink\_pk\_ZCD}$ | Max. output sink peak current | ZCD comparator triggered turn-off(3) | - | 4 | - | A |
| $t_r$ | Rise time | - | - | 140 | - | ns |
| $t_f$ | Fall time (OFF comparator) | OFF comparator triggered turn-off | - | 80 | - | ns |
| $t_{f\_ZCD}$ | Fall time (ZCD comparator) | ZCD comparator triggered turn-off | - | 30 | - | ns |
| $V_{GDclamp}$ | Output clamp voltage | $I_{GD}$ = -5 mA; $V_{CC}$ = 20 V; SRK2001/TR | 9 | 11 | 13 | V |
| $V_{GDL\_UVLO}$ | UVLO saturation | $V_{CC}$ = 0 to $V_{CC\_On}$, $I_{sink}$ = 5 mA | - | 1 | 1.3 | V |

1. *Parameters tracking each other.*
2. *Low consumption mode is one of the following: automatic sleep mode, converter burst mode detect or EN pin pulled low.*
3. *Parameter guaranteed by design.*

# 7 Operation description

The device block diagram is shown in Figure 1. The SRK2001 can be supplied through the VCC pin by the same converter output voltage, within a wide voltage range (from 4.5 V to 32 V), internally clamped to $V_{CCZ}$ (36 V typical). An internal UVLO (undervoltage lockout) circuit with hysteresis keeps the device switched off at supply voltage lower than the turn-on level $V_{CC\_On}$, with reduced consumption.

After the startup, the operation with $V_{CC}$ floating (or disconnected by supply voltage) while pins DVS1,2 are switching is not allowed: this in order to avoid that a dV/dt on the DVS pin causing a high flowing current with possible damage to the IC.

The core of the device is the control logic block, implemented by asynchronous logic: this digital circuit generates the logic signals to the output drivers, so that the two external power MOSFET are switched on and off, depending on the evolution of their drain-source voltages, sensed on the DVS-SVS pin pairs through the comparators block.

The logic that controls the driving of the two SR MOSFET is based on two gate-driver state machines working in parallel in an interlocked way to avoid switching on both gate drivers at the same time. A third state machine manages the transitions from the normal operation to sleep mode and vice versa.

## 7.1 Drain voltage sensing

The SRK2001 basic operation is such that each synchronous rectifier MOSFET is switched on whenever the corresponding transformer half-winding starts conducting (i.e., when the MOSFET body diode, or an external diode in parallel, starts conducting) and it is then switched off when the flowing current approaches zero. To understand the polarity and the level of this current, the IC is provided with two pairs of pins (DVS1-SVS1 and DVS2-SVS2) that sense the drain-source voltage of either MOSFET (Kelvin sensing). In order to limit dynamic current injection in any condition, at least 100 Ω resistors in series to DVS1,2 pins must be used.

Referring to the typical waveforms in Figure 5, there are three significant voltage thresholds: the first one, $V_{TH\_A}$ (= 1.4 V), sensitive to positive-going edges, arms the opposite gate driver (interlock function). The second one, $V_{TH\_PT}$ (= 0.7 V), sensitive to negative-going edges provides a pre-trigger of the gate driver; the third one $V_{TH\text{-}ON}$ is the (negative) threshold that triggers the gate driver as the body diode of the SR MOSFET starts conducting.

## 7.2 Turn-on

The turn-on logic is such that each SR MOSFET is switched on when the sensed drain- source voltage goes below the $V_{TH\_ON}$ threshold: to avoid false triggering of the gate driver, an adaptive masking delay $T_{D\_On}$ is introduced. This delay assumes a minimum value at the high load and increases with decreasing load levels. The aim of $T_{D\_On}$ is to avoid a premature turn-on at lower load conditions, triggered by capacitive currents (due to secondary side parasitic capacitance and not really related to the current flowing through the MOSFET body diode.

**Figure 5. Typical waveforms**

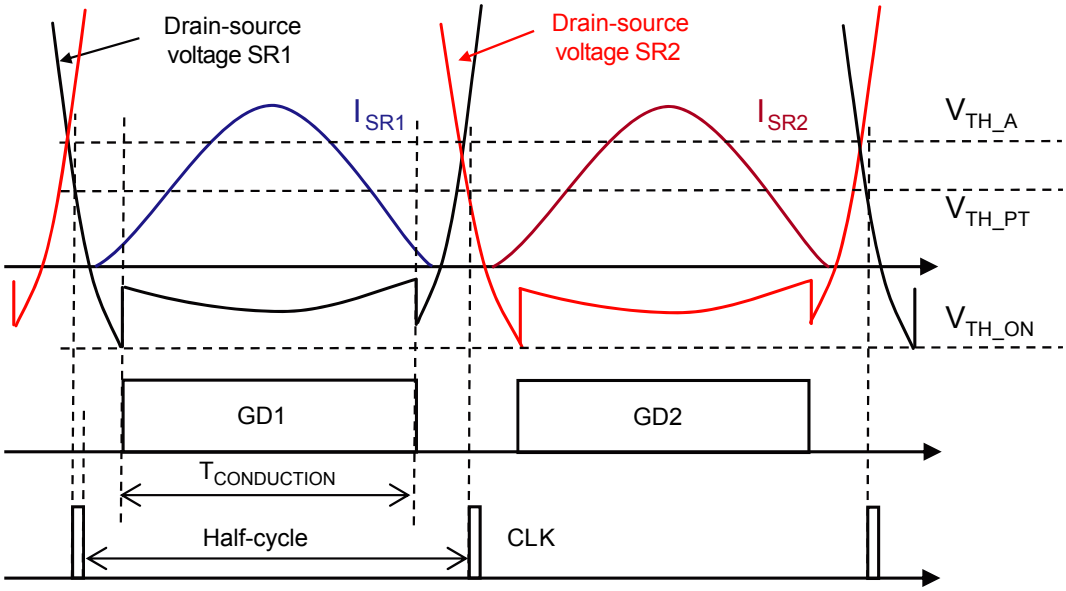



Figure 6 shows the effect of this parasitic: in case at the reduced load a capacitive current spike should trigger the turn-on, there would be a current inversion (flowing from the output capacitor toward the SR MOSFET). This current inversion would cause a discharge of the output capacitor and consequently an increase of the rectified current rms value, in order to balance that discharge; this in turn would affect the converter efficiency. Therefore, the adaptive turn-on delay is aimed to maximize the efficiency in each load operating condition. Figure 7 shows the turn-on at the full load with minimum delay (TD_On_min) and at the reduced load with increased delay (up to TD_On.max equal to 40% of the clock cycle).

**Figure 6. Capacitive current spike effect at turn-on**

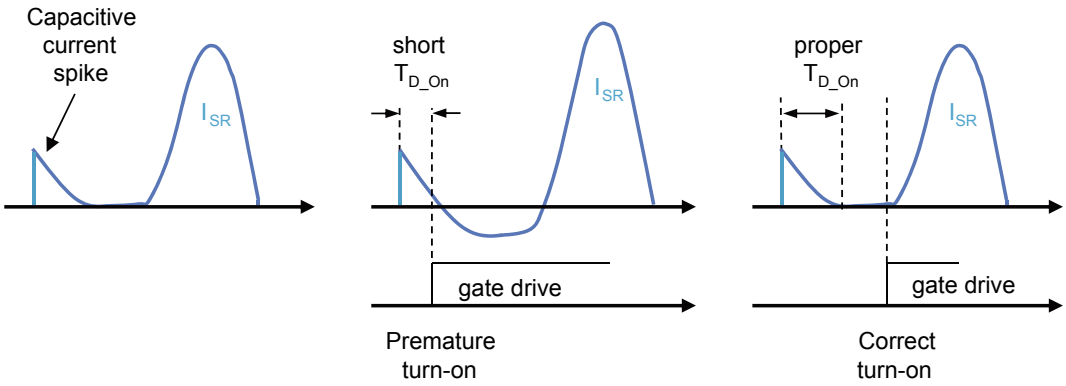
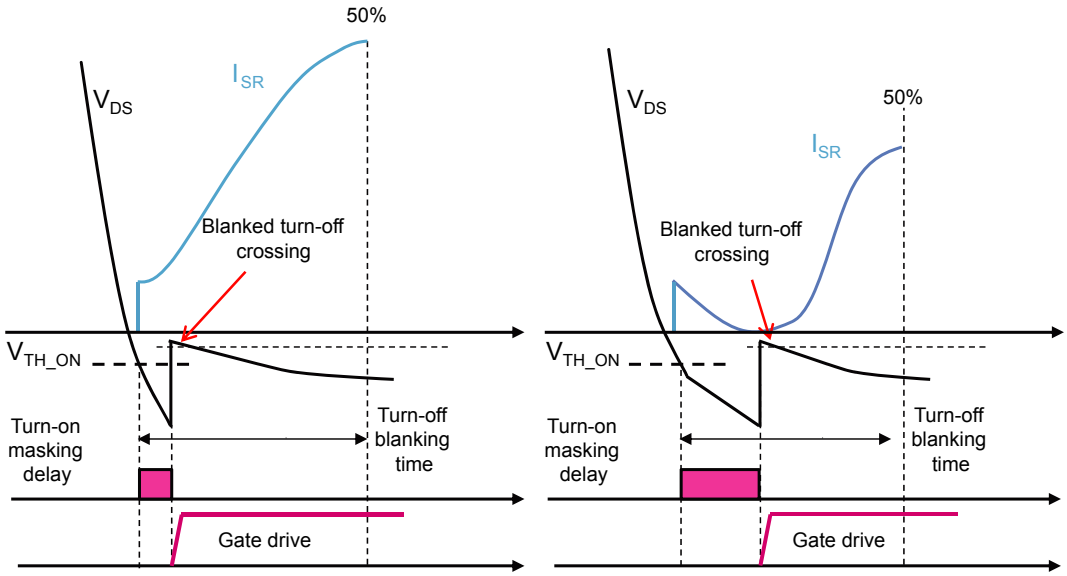


Figure 7. **Full load and light load turn-on**




At the startup and on sleep mode exit, the control circuit starts with a turn-on delay set to 30% of the clock cycle and progressively adapts it to the proper value. This allows reducing system perturbation both during the startup and while exiting the sleep mode during a fast zero to full load transition. After the turn-on, a blanking time (equal to 50% of the clock period) masks an undesired turn-off due to the drain-source voltage drop, consequent to MOSFET switch on (flowing current passes from the body diode to MOSFET channel resistance).

## 7.3 Adaptive turn-off

The SR MOSFET turn-off may be triggered by an adaptive turn-off mechanism (two slope turn-off) or by the ZCD_OFF comparator (fast turn-off, see Section 7.4).

Due to the stray inductance in series with the SR MOSFET $R_{DS(on)}$ (mainly the package stray inductance), the sensed drain-source signal is not really equal to the voltage drop across the MOSFET $R_{DS(on)}$, but it anticipates the time instant where the current reaches zero, causing a premature MOSFET turn-off.

To overcome this problem (without adding any stray inductance compensation circuit), the device uses a turn-off mechanism based on an adaptive algorithm that turns off the SR MOSFET when the sensed drain voltage reaches zero adapting progressively the turn-off to the maximum conduction period.

Figure 8. **Adaptive turn-off**

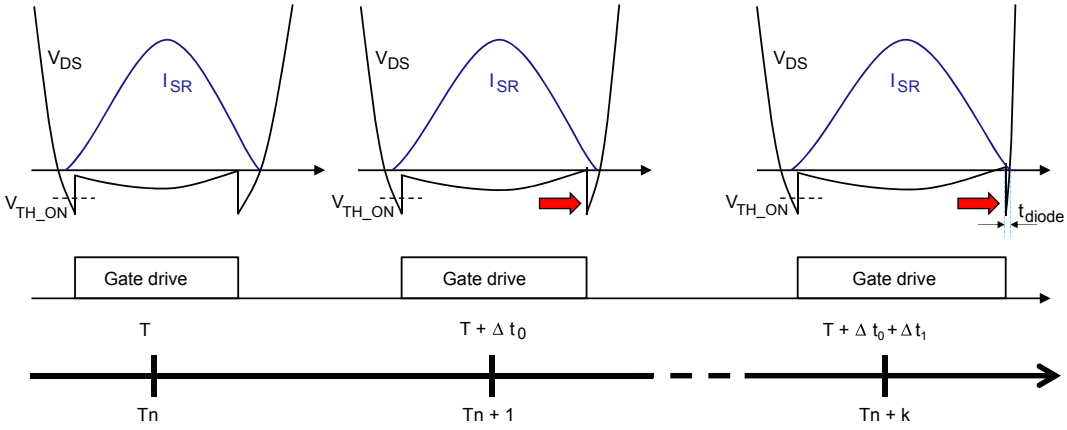



Figure 8 shows this adaptive algorithm: cycle-by-cycle the conduction time is maximized, allowing in a steady-state the maximum converter efficiency.

During the startup and on sleep mode exit, the control circuit turns off the SR MOSFET at 50% of the clock cycle and progressively adapts this delay in order to maximize the SR MOSFET conduction time to help reduce system perturbations.

## 7.4 ZCD comparator

The IC is equipped with a ZCD comparator that is always ready to quickly turn-off the SR MOSFET to avoid current inversion that would cause SR MOSFET failure and even half bridge destruction, if the primary controller not equipped with proper protections.

The ZCD (zero current detection) comparator acts during fast load transitions or the short-circuit operation and when the above resonance operation occurs. It senses that the current has reached the zero level and triggers the gate drive circuit for a very fast MOSFET turn-off (with a total delay time $T_{D\_Off}$).

The ZCD comparator threshold is not fixed but self-adaptive.

In the steady-state load operation and in case of slow load transitions, the turn-off is prevalently managed by the adaptive mechanism (characterized by the two slope turn-off driving). Instead, during fast transitions or during above resonance operation, the ZCD_OFF comparator will take over, causing a fast MOSFET switch-off that prevents undesired current inversions.

The ZCD_OFF comparator is blanked for 450 ns after the turn-on.

Depending on SR MOSFET choice, some premature turn-off triggered by the ZCD_OFF comparator may be found due to the noise present on the drain-source sensed signal: this is worse with lower $R_{DS\_ON}$ (due to worse signal to noise ratio) and lower stray inductance of the MOSFET package. Normally the load level where this may happen is such that the circuit has already entered a low consumption state (for example in burst mode from primary controller); if this is not the case, some noise reduction may be helpful, for example by using RC snubbers across the SR MOSFET drain-source.

## 7.5 Gate drive

The IC is provided with two high current gate-drive outputs, each capable of driving one or more N-channel power MOSFET in parallel.

The high-level voltage provided by the driver is clamped at $V_{GDclamp}$ in order to avoid excessive voltage levels on the gate in case the device is supplied with a high $V_{CC}$, thus minimizing the gate charge provided in each switching cycle.

The two gate drivers have a pull-down capability that ensures the SR MOSFET cannot be spuriously turned on even at low $V_{CC}$: in fact, the drivers have a 1 V (typ.) saturation level at $V_{CC}$ below the turn-on threshold.

As described in the previous paragraphs, either the SR MOSFET is switched on after the current starts flowing through the body diode, when the drain-source voltage is already low (equal to $V_F$); therefore there is no Miller effect nor switching losses at the MOSFET turn-on, in which case the drive doesn't need to provide a fast turn-on.

Also at the turn-off, during steady-state load conditions, when the decision depends on the adaptive control circuitry, there is no need to have a very fast drive with hard pull-down because the current has not yet reached zero and the operation is far from the current inversion occurrence. Moreover, slow transitions also help reduce the perturbation introduced into the system that arise due to the MOSFET turn-on and turn-off, contributing to improve the overall behavior of the LLC resonant converter.

The gate-drive circuit is specifically designed to reduce the switching noise at the turn-off, due to parasitic inductance in the driving current path. In fact, during the adaptive turn-off, it provides a controlled turn-off time (with the characteristic two-slope falling edge) in order to limit the current peak during gate drive transition, and does not require any resistor in series to the SR MOSFET gates.

On the other side, during very fast load transitions or the short-circuit operation, when the turn-off decision is taken by ZCD logic, the MOSFET turn-off needs to be very fast to avoid current inversion: therefore the two gate drivers are designed to guarantee for a very short turn-off total delay $T_{D\_Off}$.

The SR mosfet is not turned on at cycle “n+1” when the conduction period at cycle “n” becomes lower than the 60% of the switching period at cycle “n-1”. The conduction period and the switching period are internally estimated by the IC looking at the DVS signals. The former correspond to the time from one pre-trigger event to the next arming event. The latter correspond to the time between two consecutive pre-trigger events.

## 7.6 Intelligent automatic sleep mode

A unique feature of this IC is its intelligent automatic sleep mode. The logic circuitry is able to detect a light-load condition for the converter and stop gate driving, reducing also the IC quiescent consumption. This improves converter efficiency at the light-load, where the power losses on the rectification body diodes (or external diodes in parallel to the MOSFET) become lower than the power losses in the MOSFET and those related to their driving. The IC is also able to detect an increase of the converter's load and automatically restarts gate driving.

The algorithm used by the intelligent automatic sleep mode is based on a dual time measurement system: the duration of the half-switching period (i.e., the clock cycle in Figure 5) and the duration of the conduction time of the synchronous rectifier.

The duration of a clock cycle is measured from the falling edge of a clock pulse to the rising edge of the subsequent clock pulse; the duration of the SR MOSFET conduction is measured from the moment its body diode starts conducting (drain-source voltage falling below $V_{TH-ON}$) to the moment the gate drive is turned off, in case the device is operating, or to the moment the body diode ceases to conduct (drain-to-source voltage going above $V_{TH-ON}$) during the sleep mode operation. While at the full load the SR MOSFET conduction time occupies almost 100% of the half-switching cycle, as the load is reduced, the conduction duty cycle is reduced and, as it falls below DOFF (see data in Table 4), the device enters the sleep mode. To prevent wrong decisions, the sleep mode condition must be confirmed for 512 consecutive clock cycles.

Once in the sleep mode, SR MOSFET gate driving is re-enabled when the conduction duty cycle of the body diode (or the external diodes in parallel to the MOSFET) exceeds DON: the number of clock cycles needed to exit the sleep mode is proportional to the difference between the body diode conduction duty cycle and the programmed DON threshold. This allows a faster sleep-out in case of the heavy load transient low-to-high.

Furthermore, in order to reduce the perturbation introduced by a sudden sleep mode state entering, a soft-sleep transition procedure is adopted, that progressively decreases the conduction time before entering the sleep mode state.

After entering the sleep mode, timing is ignored for 8 switching cycles respectively to let the resulting transient in the output current fade-out, then the timing check is enabled.

The automatic sleep mode function can be disabled by keeping the EN pin open at startup (see Section 7.8). This may be beneficial to the overall system behavior in case of conflict with the burst mode operation of the half-bridge converter driven by the primary controller. When automatic sleep mode is disabled, the SRK2001 can enter low consumption state (during which SR MOSFETs cannot be turned on) when it recognizes an interruption in the switching activity by the primary controller.

## 7.7 Burst-mode operation

Normally, at reduced loads, resonant converters enter burst mode operation in order to increase converter efficiency. The SRK2001 detects that the primary controller has stopped switching and enters its low consumption state. The condition to detect burst mode operation is that both DVS1,2 pins are above the arming voltage $V_{TH\_A}$ for at least 20 µs (typ).

After the primary controller restarts switching, the SRK2001 resumes operation when it detects that the conduction duty cycle has increased above the value $D_{ON\_BM}$ programmed by the user through a proper choice of the RPG resistor (see Table 7). The number of clock cycles needed to exit burst mode is proportional to the difference between the body diode conduction duty cycle and the programmed $D_{ON}$ threshold: this allows a faster sleep-out in case of the heavy load transient low-to-high. After recognizing that the conduction duty cycle is longer than the programmed $D_{ON}$, 12 switching cycles (i.e., 24 clock cycles) are still needed before the SRK2001 restarts driving the SR MOSFET (in order to allow the settlement of the internal timers, lost during the low consumption state, where most of the internal circuitry was not supplied or turned off).

## 7.8 EN and PROG pins: function and usage

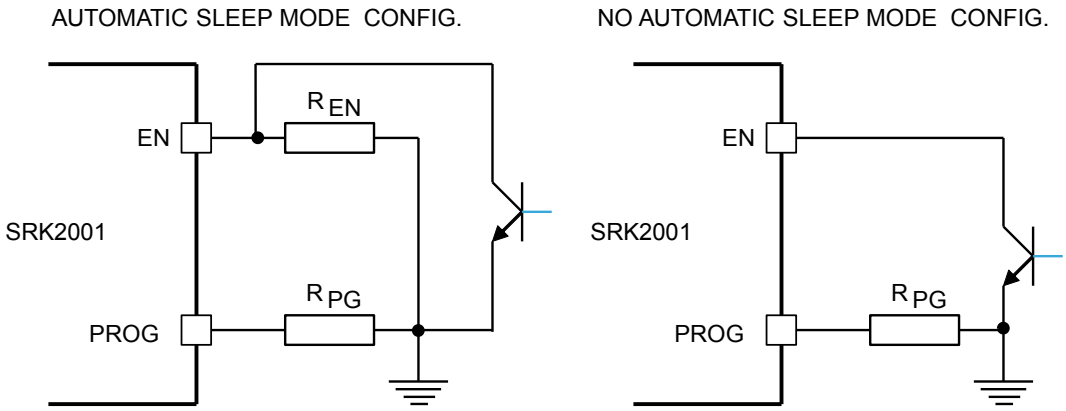
The EN pin and PROG pin allow the user to configure two different operating modes:

- Automatic sleep mode function enabled (described in Section 7.6)
- Automatic sleep mode function disabled

The configuration is set when the $V_{CC}$ supply voltage rises above the turn-on threshold $V_{CC\_ON}$ and the EN pin voltage is higher than the enable threshold ($V_{EN\_ON}$): during this pin-strap phase, the voltages on EN and PROG pins are detected and the corresponding values of $D_{ON}$ and $D_{OFF}$ (see Table 5 and Table 6) are internally stored as long as $V_{CC}$ is within the supply range and EN pin voltage is above the disable threshold ($V_{EN\_OFF}$).

During normal operation the EN pin can be used as remote on-off input, using a small signal transistor connected to the pin, as shown in Figure 9: when the switch is closed, the pin voltage goes below the $V_{EN\_OFF}$ threshold, the controller stops operating and enters a low consumption state; it resumes the operation when the switch is opened and the pin voltage surpasses the $V_{EN\_ON}$ threshold. With $V_{CC}$ supply in the operating range, the pinstrap phase is repeated each time that the EN pin is driven low to high (above the $V_{EN\_ON}$ threshold) during user remote ON-OFF.

Figure 9. **EN - PROG pin configurations**




### 7.8.1 Automatic sleep mode function enabled

Automatic sleep mode is enabled when a resistor equal or below 180 kΩ is connected from the EN pin to GND during the startup phase (see Figure 9).

During the startup phase (when the external NPN switch has to be kept open), an internal current generator $I_{EN}$ is enabled: its current is sourced to the EN pin and sets the voltage across the external resistor $R_{EN}$. By using a resistance value equal or below 180 kΩ, the voltage stays below the internal threshold and the automatic sleep mode function is enabled. The voltage level (i.e. the resistance value) also sets the conduction time (in terms of duty cycle) below which the SRK2001 enters sleep mode (see Table 5 and Table 6, $D_{OFF}$ column). The configuration is internally stored and then the internal current generator $I_{EN}$ is decreased to $I_{EN\_run}$.

At the same time, during the startup phase, another internal current generator $I_{PROG}$ is enabled: its current is sourced to the PROG pin and sets the voltage across the external resistor $R_{PG}$. Depending on this voltage level, the conduction time (in terms of duty cycle) above which the SRK2001 exits from sleep mode is set (see Table 5 and Table 6, $D_{ON}$ column). This configuration is internally stored and then the internal current generator $I_{PROG}$ is disabled.

The lookup tables show the allowed conduction time combinations, depending on $R_{EN}$ and $R_{PG}$ values (1% tolerance resistors are recommended).

Table 5. **Lookup table I: $R_{EN}$ = 100 kΩ**

| $D_{OFF}$ | $D_{ON}$ | $R_{PG}$ |
|---|---|---|
| 40% | 80% | $R_{PG}$ = 0 Ω |
| | 75% | $R_{PG}$ = 100 kΩ |
| | 65% | $R_{PG}$ = 180 kΩ |
| | 60% | $R_{PG}$ open |

Table 6. **Lookup table II: $R_{EN}$ = 180 kΩ**

| $D_{OFF}$ | $D_{ON}$ | $R_{PG}$ |
|---|---|---|
| 25% | 75% | $R_{PG}$ = 0 Ω |
| | 70% | $R_{PG}$ = 100 kΩ |
| | 60% | $R_{PG}$ = 180 kΩ |
| | 55% | $R_{PG}$ open |

### 7.8.2 Automatic sleep mode function disabled

Automatic sleep mode is disabled when the EN pin is open during startup phase (see Figure 9).

During the startup phase (when the external NPN switch is open), an internal pull-up brings the EN pin to a voltage above the internal threshold so that the automatic sleep mode function is disabled. The configuration is internally stored.

At the same time, during the startup phase, another internal current generator $I_{PROG}$ is enabled: its current is sourced to the PROG pin and sets the voltage across the external resistor $R_{PG}$. Depending on this voltage level, the conduction time (in terms of duty cycle) above which the SRK2001 exits from low consumption state, resuming normal operation, is set (see Table 7). This configuration is internally stored and then the internal current generator $I_{PROG}$ is disabled.

When automatic sleep mode is disabled, the SRK2001 can no longer enter the low consumption state if the conduction duty cycle reduces, because of reduced load. However, the SRK2001 recognizes burst mode operation by the primary controller (or an external turn-off command on the EN pin). When half-bridge switching is stopped, the SRK2001 detects burst mode operation and enters the low consumption state, during which SR MOSFET cannot be turned on (see Section 7.7). As the primary controller restarts switching (or the EN pin goes back high), the SRK2001 resumes the operation when it detects that the conduction duty cycle has increased above the value DON_BM programmed by the user through a proper choice of the RPG resistor as summarized in Table 7.

**Table 7. Lookup table I: $R_{EN}$ = 100 kΩ**

| $D_{ON\_BM}$ | $R_{PG}$ |
|---|---|
| 80% | $R_{PG}$ = 0 Ω |
| 75% | $R_{PG}$ = 100 kΩ |
| 65% | $R_{PG}$ = 180 kΩ |
| 0% | $R_{PG}$ open |

## 7.9 Layout guidelines

The GND pin is the return of the bias current of the device and return for gate drive currents: it should be routed to the common point where the source terminals of both synchronous rectifier MOSFET are connected. When laying out the PCB, care must be taken in keeping the source terminals of both SR MOSFET as close to one another as possible and routing the trace that goes to the GND separately from the load current return path. This trace should be as short as possible and be as close to the physical source terminals as possible. Keeping the layout as geometrically symmetrical as possible will help render circuit operation electrically symmetrical.

Also drain-source voltage sensing should be performed as physically close to the drain and source terminals as possible in order to minimize the stray inductance involved by the load current path that is in the drain-to-source voltage sensing circuit.

The use of bypass capacitors between the $V_{CC}$ and GND is recommended. They should be low-ESR, low-ESL type and located as close to the IC pins as possible. Sometimes, a series resistor (in the tens of ohms) between the converter output voltage and the $V_{CC}$ pin, forming an RC filter along with the by-pass capacitor, can help obtain a cleaner $V_{CC}$ voltage.

# 8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 8.1 SSOP10 package information

**Figure 10. SSOP10 package outline**

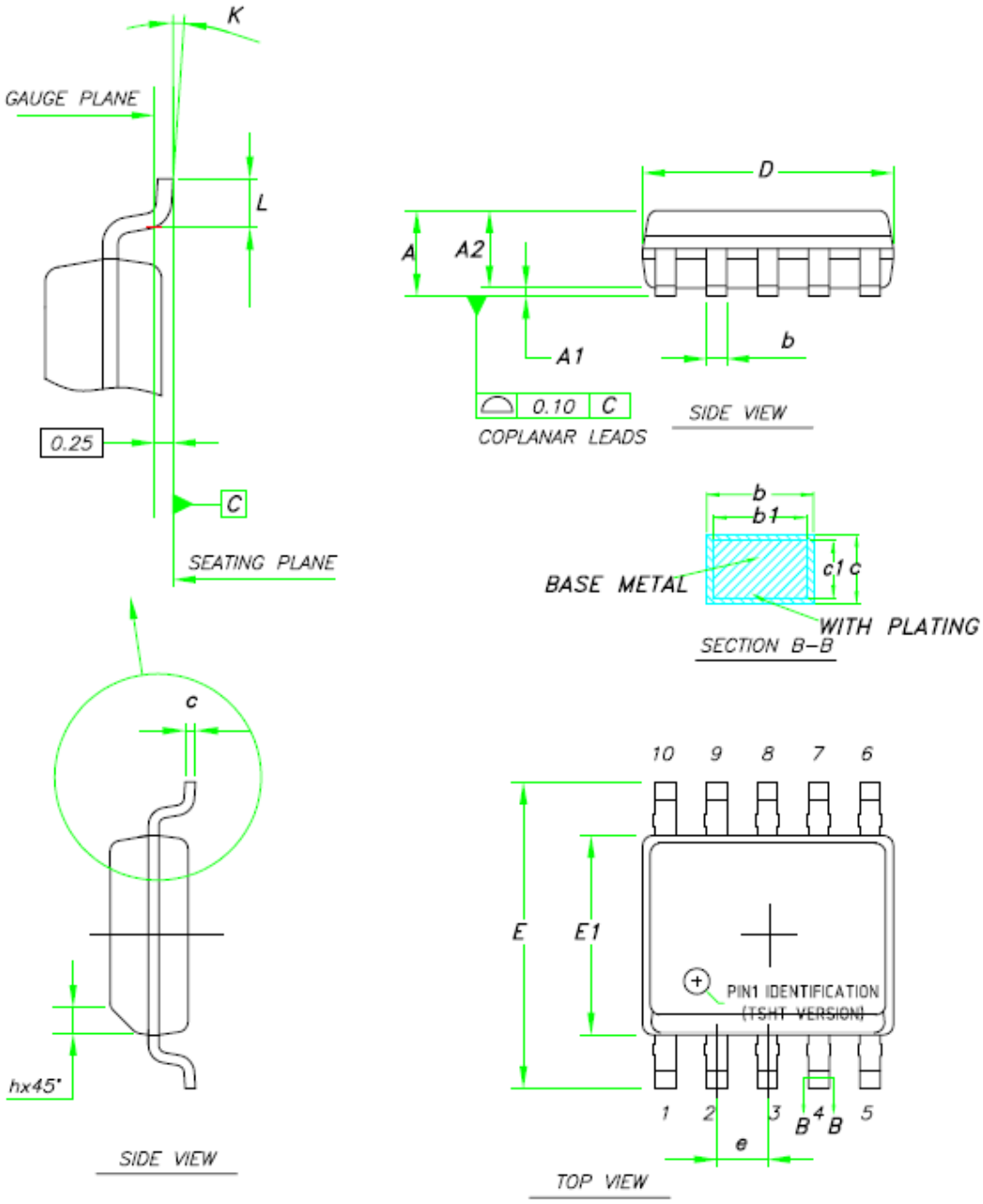


Table 8. **SSOP10 package mechanical data**

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 1.75 |
| A1 | 0.10 | - | 0.225 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.39 | - | 0.47 |
| b1 | 0.38 | 0.41 | 0.44 |
| c | 0.20 | - | 0.24 |
| c1 | 0.19 | 0.20 | 0.21 |
| D | 4.80 | 4.90 | 5 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.00 BSC | | |
| h | 0.25 | - | 0.50 |
| L | 0.50 | - | 0.80 |
| K | 0° | - | 8° |

# 9 Ordering information

Table 9. **Ordering information**

| Order code | Package | Packing |
|---|---|---|
| SRK2001 | SSOP10 | Tube |
| SRK2001TR | | Tape and reel |

## Revision history

Table 10. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 16-Jan-2015 | 1 | Initial release. |
| 09-Feb-2015 | 2 | Updated Table 5 on page 7 (updated "$V_{GDclamp}$" - SRK2001L/LTR -removed "$R_{GATE}$ = 5.6 Ω", removed min. and max. values). |
| 12-May-2015 | 3 | Updated Section 5.5 on page 13.<br>Minor modifications throughout document. |
| 14-Feb-2017 | 4 | Removed "SRK2001L/LTR" and "logic level MOSFETS" from Features, Table 1, Table 2, Table 5, and Section 5.5.<br>Minor modifications throughout document. |
| 6-Sept-2018 | 5 | Updated Section 5.6<br>Added Section 5.7: Burst mode operation<br>Updated Section 5.8: EN and PROG pins: function and usage |
| 02-Sep-2021 | 6 | Throughout document:<br>• updated document template<br>• Section, figure and table indexes moved to bottom of document<br>• minor text edits<br>Old Section 1 "Block diagrams and pin connections" split into:<br>• Section 1: Block diagrams<br>• Section 2: Pin connections and functions<br>Old Section 2 Maximum ratings" split into:<br>• Section 3: Absolute maximum ratings<br>• Section 4: Thermal data<br>In Section 7.1: Drain voltage sensing:<br>• Added new paragraphs, starting with "Depending on the configuration of pins PROG and EN..."<br>In Section 7.7: Burst-mode operation:<br>• Removed sentence from "For the correct operation of the SRK2001..." to "...it is recommended to keep the PROG pin open"<br>In Section 7.8: EN and PROG pins: function and usage:<br>• Updated paragraph "The configuration is set ..."<br>• Replaced sentence "The small signal transistor has to be …" with "With $V_{CC}$ supply in the operating range..."<br>In Section 8.1: SSOP10 package information:<br>• updated Section 8.1: SSOP10 package information<br>• updated Table 8. SSOP10 package mechanical data |
| 28-Apr-2026 | 7 | Updated cover image and removed "Product Summary" table.<br>Updated Section 7.1: Drain voltage sensing: removed last paragraph.<br>Updated Section 7.5: Gate drive.<br>Added Section 9: Ordering information.<br>In Section 8.1: updated Figure 10. SSOP10 package outline. |

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