

Single Input Buffer

NL17SZ16

The NL17SZ16 is a single input Buffer in tiny footprint packages.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.4 ns t_{PD} at $V_{CC} = 5$ V (typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in SC-88A, SC-74A-5 and SOT-553-5 Packages
- Chip Complexity < 100 FETs
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

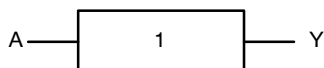
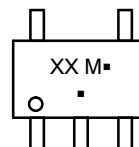


Figure 1. Logic Symbol

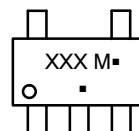
MARKING DIAGRAMS



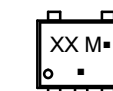
SC-88A
DF SUFFIX
CASE 419A-02



SC-74A-5
DBV SUFFIX
CASE 318BQ



SOT-553-5
XV5 SUFFIX
CASE 463B



XX = Specific Device Code
M = Date Code*
■ = Pb-Free Package

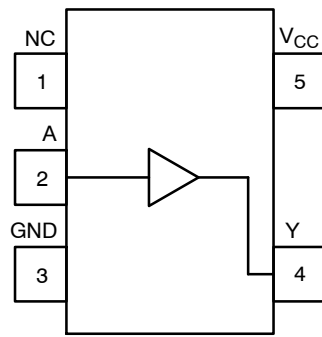
(Note: Microdot may be in either location)

* Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

NL17SZ16



(SC-88A/SOT-553-5/SC-74A-5)

Figure 2. Pinout (Top View)

PIN ASSIGNMENT

(SC-88A/SOT-553-5/SC-74A-5)

Pin	Function
1	NC
2	A
3	GND
4	Y
5	V _{CC}

FUNCTION TABLE

A Input	Y Output
L	L
H	H

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to +6.5	V
V_{OUT}	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	-50	mA
I_{OUT}	DC Output Source/Sink Current	± 50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2) SC-88A SC-74A-5 SOT-553-5	377 320 324	°C/W
P_D	Power Dissipation in Still Air SC-88A-5 SC-74A SOT-553-5	332 390 386	mW
MSL	Moisture Sensitivity	Level 1	-
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device's lifespan or reliability.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	5.5	V
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	0 0 0	V_{CC} 5.5 5.5	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise and Fall Time $V_{CC} = 1.65$ V to 1.95 V $V_{CC} = 2.3$ V to 2.7 V $V_{CC} = 3.0$ V to 3.6 V $V_{CC} = 4.5$ V to 5.5 V	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25\text{ }^{\circ}\text{C}$			$-55\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$		Units
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65 to 1.95	$0.65 \times V_{CC}$			$0.65 \times V_{CC}$		V
			2.3 to 5.5	$0.70 \times V_{CC}$			$0.70 \times V_{CC}$		
V_{IL}	Low-Level Input Voltage		1.65 to 1.95			$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
			2.3 to 5.5			$0.30 \times V_{CC}$		$0.30 \times V_{CC}$	
V_{OH}	High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -100\text{ }\mu\text{A}$ $I_{OH} = -4\text{ mA}$ $I_{OH} = -8\text{ mA}$ $I_{OH} = -12\text{ mA}$ $I_{OH} = -16\text{ mA}$ $I_{OH} = -24\text{ mA}$ $I_{OH} = -32\text{ mA}$	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	$V_{CC} - 0.1$ 1.29 1.9 2.2 2.4 2.3 3.8	V_{CC} 1.4 2.1 2.4 2.7 2.5 4.0	– – – – – – –	$V_{CC} - 0.1$ 1.29 1.9 2.2 2.4 2.3 3.8	– – – – – – –	V
V_{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 100\text{ }\mu\text{A}$ $I_{OL} = 4\text{ mA}$ $I_{OL} = 8\text{ mA}$ $I_{OL} = 12\text{ mA}$ $I_{OL} = 16\text{ mA}$ $I_{OL} = 24\text{ mA}$ $I_{OL} = 32\text{ mA}$	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	– – – – – – –	– 0.08 0.2 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55	– – – – – – –	0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I_{IN}	Input Leakage Current	$V_{IN} = 5.5\text{ V}$ or GND	1.65 to 5.5	–	–	± 0.1	–	± 1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{IN} = 5.5\text{ V}$ or $V_{OUT} = 5.5\text{ V}$	0	–	–	1.0	–	10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	–	–	1.0	–	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

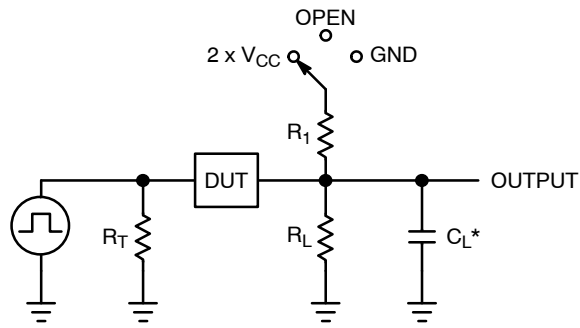
Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25 °C			-55 °C ≤ T _A ≤ 125 °C		Units
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay, A to Y (Figures 3 and 4)	R _L = 1 MΩ, C _L = 15 pF	1.65 to 1.95	–	5.3	11.4	–	12.0	ns
		R _L = 1 MΩ, C _L = 15 pF	2.3 to 2.7	–	2.9	6.5	–	7.0	
		R _L = 1 MΩ, C _L = 15 pF	3.0 to 3.6	–	2.1	4.5	–	4.7	
		R _L = 500 Ω, C _L = 50 pF		–	2.9	5.0	–	5.2	
		R _L = 1 MΩ, C _L = 15 pF	4.5 to 5.5	–	1.8	3.9	–	4.1	
		R _L = 500 Ω, C _L = 50 pF		–	2.4	4.3	–	4.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V _{CC} = 3.3 V, V _{IN} = 0 V or V _{CC} 10 MHz, V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	9 11	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Figure 3. Test Circuit

Test	Switch Position	C_L , pF	R_L , Ω	R_1 , Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	$2 \times V_{CC}$	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care

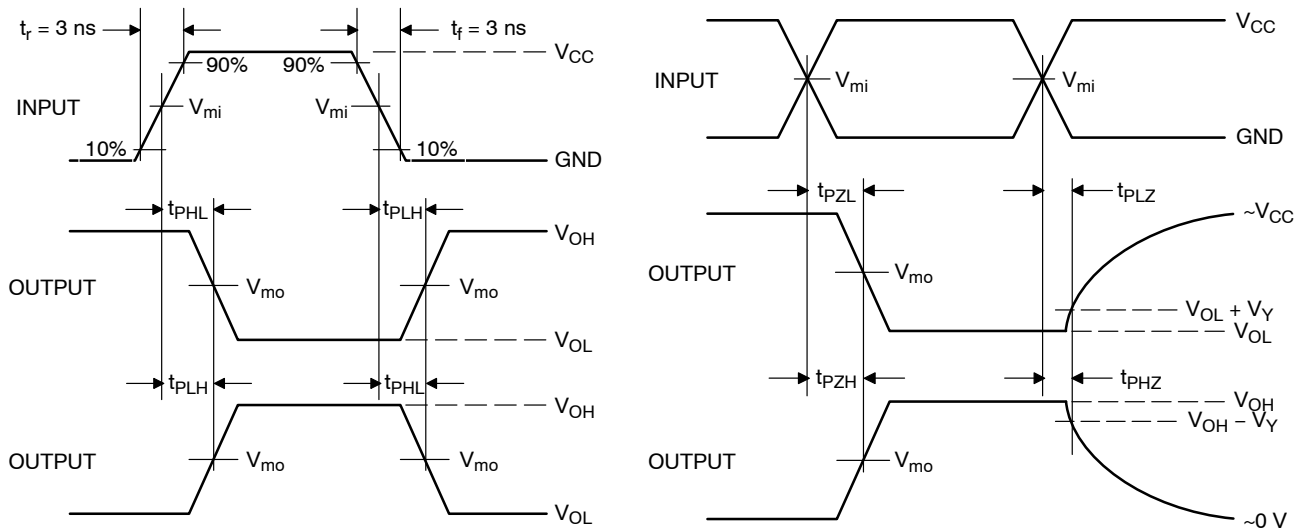


Figure 4. Switching Waveforms

V_{CC} , V	V_{mi} , V	V_{mo} , V		V_Y , V
		t_{PLH}, t_{PHL}	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

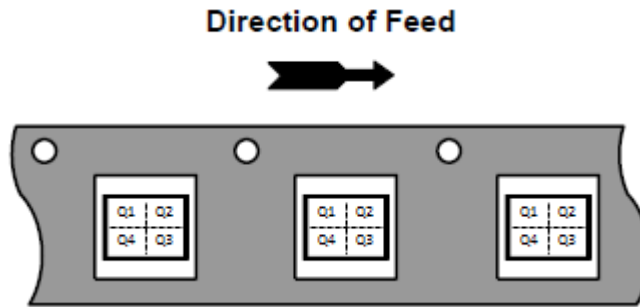
NL17SZ16

DEVICE ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
NL17SZ16DFT2G	SC-88A	LR	Q4	3000 / Tape & Reel
NL17SZ16DBVT1G	SC-74A-5	AL	Q4	3000 / Tape & Reel
NL17SZ16XV5T2G	SOT-553-5	LR	Q4	4000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

PIN 1 ORIENTATION IN TAPE AND REEL



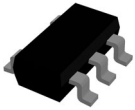
NL17SZ16

REVISION HISTORY

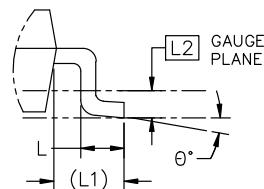
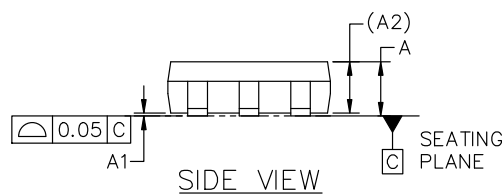
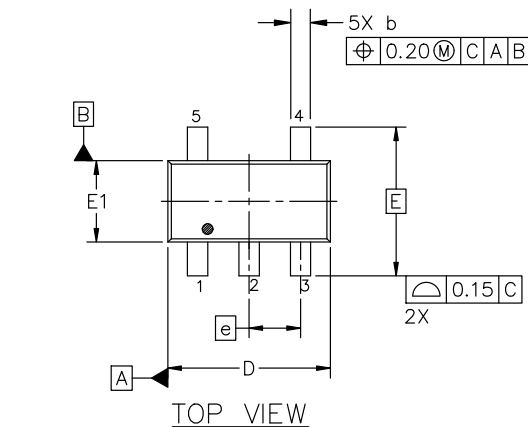
Revision	Description of Changes	Date
17	Removed the case outlines 527AE, 517AQ, 517BX and OPNs NL17SZ16DFT2G-Q, NL17SZ16P5T5G, NL17SZ16MU1TCG, NL17SZ16MU3TCG from the document.	1/27/2026

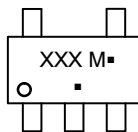
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.




SC-74A-5 3.00x1.50x0.95, 0.95P
CASE 318BQ
ISSUE C

DATE 26 FEB 2024


DETAIL "A"
SCALE 2:1

**GENERIC
MARKING DIAGRAM***


XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

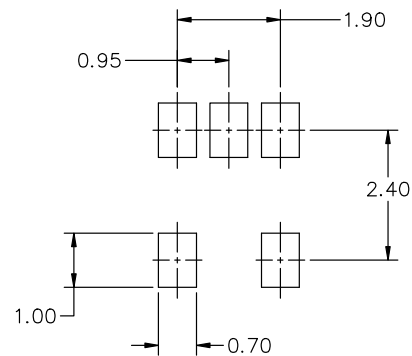
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.01	0.18	0.10
A2	0.95 REF.		
b	0.25	0.37	0.50
c	0.10	0.18	0.26
D	2.85	3.00	3.15
E	2.75 BSC		
E1	1.35	1.50	1.65
e	0.95 BSC		
L	0.20	0.40	0.60
L1	0.62 REF.		
L2	0.25 BSC		
θ	0°	5°	10°


RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	98AON66279G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-74A-5 3.00x1.50x0.95, 0.95P	PAGE 1 OF 1

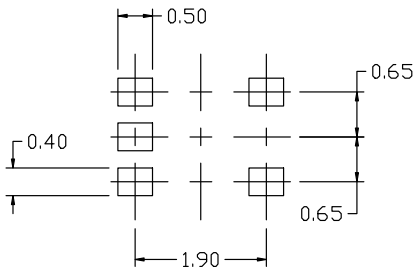
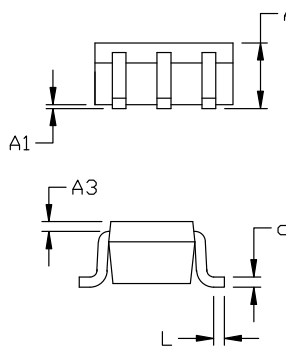
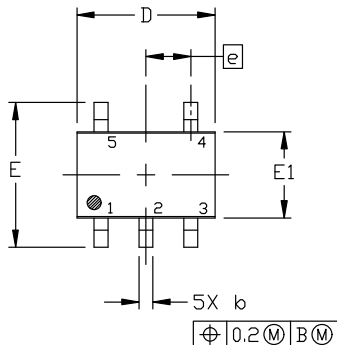
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SCALE 2:1

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE M

DATE 11 APR 2023



RECOMMENDED
MOUNTING FOOTPRINT

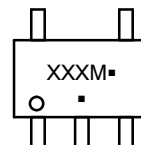
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

GENERIC MARKING
DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:

- PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:

- PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:

- PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

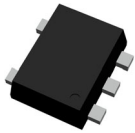
STYLE 9:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

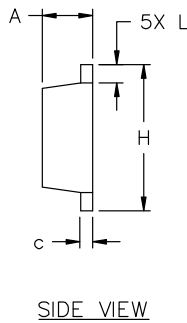
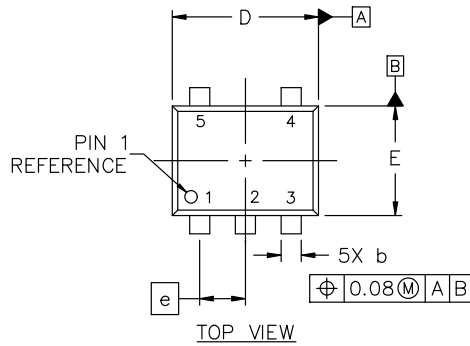
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

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SOT-553-5 1.60x1.20x0.55, 0.50P
CASE 463B
ISSUE D

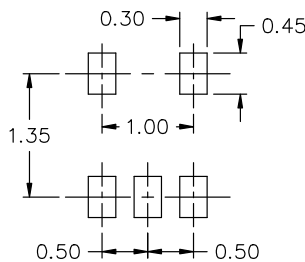
DATE 21 FEB 2024



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.55	1.60	1.65
E	1.15	1.20	1.25
e	0.50 BSC		
H	1.55	1.60	1.65
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

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STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR 1
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

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