

Three-Input AND Gate

NL17SZ11

The NL17SZ11 is a single three-input AND Gate operating from a 1.65 to 5.5 V supply.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.9 ns t_{PD} at $V_{CC} = 5$ V (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Sink 32 mA at 4.5 V
- Available in SC-74 Package
- Chip Complexity < 100 FETs
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

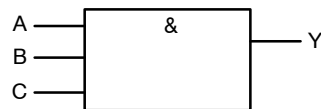


Figure 1. Logic Symbol

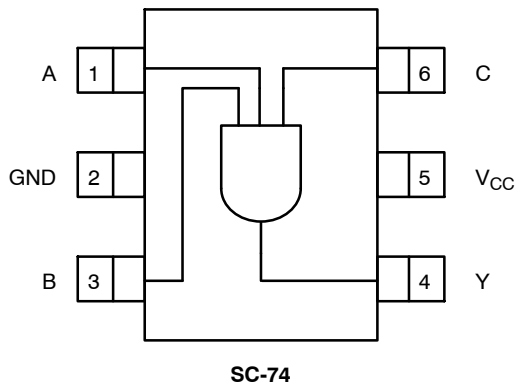
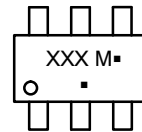


Figure 2. Pinout
(Top View)

MARKING DIAGRAM



SC-74
CASE 318F



X, XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

* Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NL17SZ11

PIN ASSIGNMENT

Pin	Function
1	A
2	GND
3	B
4	Y
5	V _{CC}
6	C

FUNCTION TABLE (Y = ABC)

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = HIGH Logic Level

L = LOW Logic Level

X = Either LOW or HIGH Logic Level

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	−0.5 to +6.5	V
V _{IN}	DC Input Voltage	−0.5 to +6.5	V
V _{OUT}	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V _{CC} = 0 V)	−0.5 to V _{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I _{IK}	DC Input Diode Current V _{IN} < GND	−50	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	−50	mA
I _{OUT}	DC Output Source/Sink Current	±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 2)	320	°C/W
P _D	Power Dissipation in Still Air	390	mW
MSL	Moisture Sensitivity	Level 1	–
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	–
V _{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Mode	2000 1000	V
I _{Latchup}	Latchup Performance (Note 4)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device's lifespan or reliability.

1. Applicable to devices with outputs that may be tri-stated.

2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.

3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.

4. Tested to EIA/JESD78 Class II.



RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V _{CC}	Positive DC Supply Voltage		1.65	5.5	V
V _{IN}	DC Input Voltage		0	5.5	V
V _{OUT}	DC Output Voltage	Active-Mode (High or Low State)	0	V _{CC}	
		Tri-State Mode (Note 1)	0	5.5	
		Power-Down Mode (V _{CC} = 0 V)	0	5.5	
T _A	Operating Temperature Range		−55	+125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 1.65 V to 1.95 V	0	20	ns
		V _{CC} = 2.3 V to 2.7 V	0	20	
		V _{CC} = 3.0 V to 3.6 V	0	10	
		V _{CC} = 4.5 V to 5.5 V	0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65 to 1.95	$0.65 V_{CC}$	–	–	$0.65 V_{CC}$	–	V
			2.3 to 5.5	$0.70 V_{CC}$	–	–	$0.70 V_{CC}$	–	
V_{IL}	Low-Level Input Voltage		1.65 to 1.95	–	–	$0.35 V_{CC}$	–	$0.35 V_{CC}$	V
			2.3 to 5.5	–	–	$0.30 V_{CC}$	–	$0.30 V_{CC}$	
V_{OH}	High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}	1.65 to 5.5	$V_{CC} - 0.1$	V_{CC}	–	$V_{CC} - 0.1$	–	V
		$I_{OH} = -100 \mu\text{A}$	1.65	1.29	1.52	–	1.29	–	
		$I_{OH} = -4 \text{ mA}$	2.3	1.9	2.1	–	1.9	–	
		$I_{OH} = -8 \text{ mA}$	3	2.5	2.8	–	2.4	–	
		$I_{OH} = -16 \text{ mA}$	3	2.4	2.68	–	2.3	–	
		$I_{OH} = -24 \text{ mA}$	4.5	3.9	4.2	–	3.8	–	
V_{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}	1.65 to 5.5	–	–	0.1	–	0.1	V
		$I_{OH} = 100 \mu\text{A}$	1.65	–	0.08	0.24	–	0.24	
		$I_{OH} = 4 \text{ mA}$	2.3	–	0.11	0.3	–	0.3	
		$I_{OH} = 8 \text{ mA}$	3	–	0.15	0.4	–	0.4	
		$I_{OH} = 16 \text{ mA}$	3	–	0.22	0.55	–	0.55	
		$I_{OH} = 24 \text{ mA}$	4.5	–	0.22	0.55	–	0.55	
I_{IN}	Input Leakage Current	$V_{IN} = 5.5 \text{ V or GND}$	1.65 to 5.5	–	–	± 0.1	–	± 1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{IN} = 5.5 \text{ V or } V_{OUT} = 5.5 \text{ V}$	0	–	–	1.0	–	10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	–	–	1.0	–	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

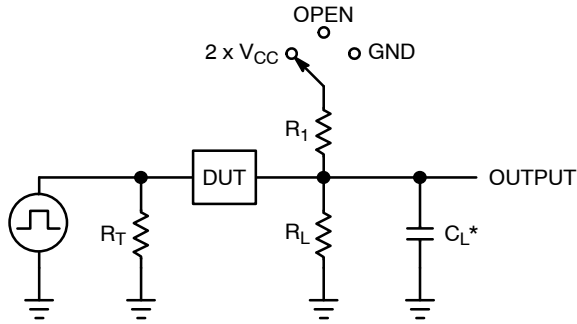
Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (A or B or C) to Y (Figure 3 and 4)	$R_L = 1 \text{ M}\Omega, C_L = 50 \text{ pF}$	1.8 ± 0.15	–	9.0	18.5	–	19.0	ns
		$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	2.5 ± 0.2	–	4.9	10.5	–	11.0	
		$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	3.3 ± 0.3	–	3.5	8.5	–	9.0	
		$R_L = 500 \Omega, C_L = 50 \text{ pF}$		–	4.1	8.5	–	9.0	
		$R_L = 1 \text{ M}\Omega, C_L = 15 \text{ pF}$	5.0 ± 0.5	–	2.5	6.5	–	7.0	
		$R_L = 500 \Omega, C_L = 50 \text{ pF}$		–	2.9	7.5	–	8.0	



CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	4.0	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	4.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit

Test	Switch Position	C _L , pF	R _L , Ω	R ₁ , Ω
t _{PLH} / t _{PHL}	Open	See AC Characteristics Table		
t _{PLZ} / t _{PZL}	2 x V _{CC}	50	500	500
t _{PHZ} / t _{PZH}	GND	50	500	500

X = Don't Care

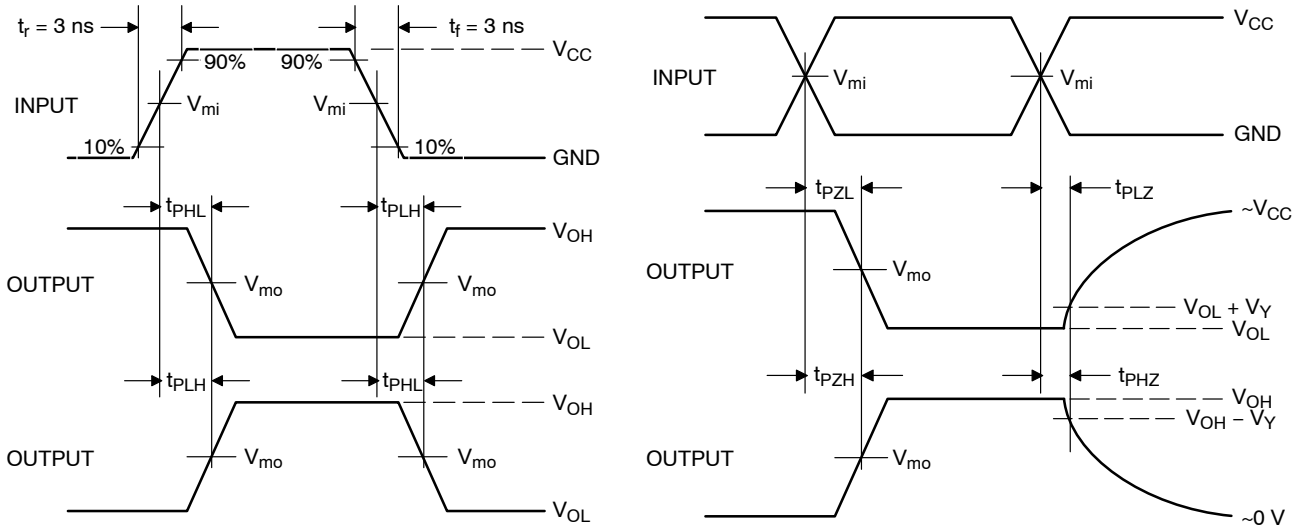


Figure 4. Switching Waveforms

V _{CC} , V	V _{mi} , V	V _{mo} , V		V _Y , V
		t _{PLH} , t _{PHL}	t _{PZL} , t _{PLZ} , t _{PZH} , t _{PHZ}	
1.65 to 1.95	V _{CC} /2	V _{CC} /2	V _{CC} /2	0.15
2.3 to 2.7	V _{CC} /2	V _{CC} /2	V _{CC} /2	0.15
3.0 to 3.6	V _{CC} /2	V _{CC} /2	V _{CC} /2	0.3
4.5 to 5.5	V _{CC} /2	V _{CC} /2	V _{CC} /2	0.3

NL17SZ11

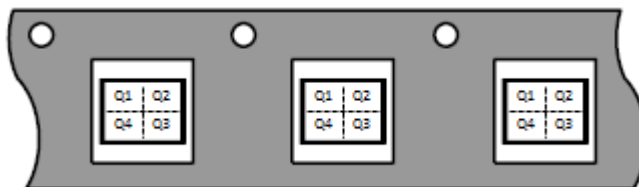
DEVICE ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
NL17SZ11DBVT1G	SC-74	AD	Q4	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

PIN 1 ORIENTATION IN TAPE AND REEL

Direction of Feed



NL17SZ11

REVISION HISTORY

2	– Rebranded the document to onsemi format. – Removed three OPNs from the Ordering Information table: NL17SZ11DFT2G, NL17SZ11MU1TCG, and NL17SZ11MU3TCG. – Deleted corresponding Case Outlines and Marking Diagrams from page 1. – Added NL17SZ11MU1TCG-Q to the Ordering Information table.	10/16/2025
3	– Updated device features and removed marking diagram CASE 517-AQ from page 1. – Deleted unused UDFN6 pin assignment from Figure 2. – Removed non-existent OPN NL17SZ11MU1TCG-Q from the ordering information table. – Removed obsolete SC-88 and UDFN6 references from the Maximum Ratings table.	1/22/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

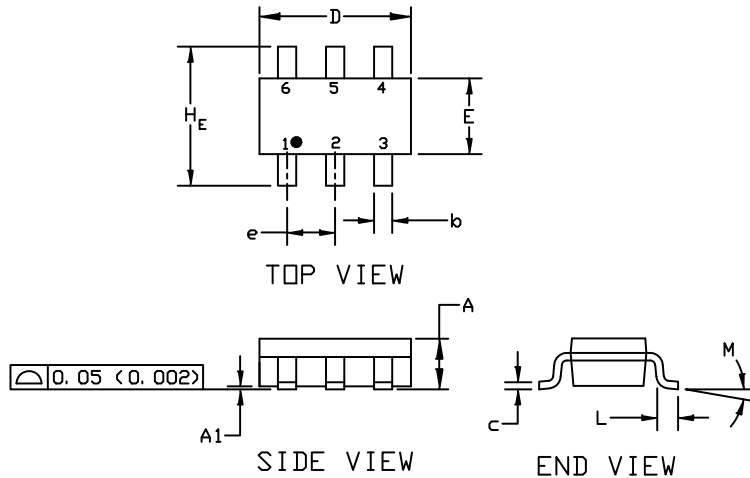




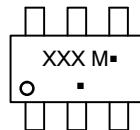
SCALE 2:1

SC-74
CASE 318F
ISSUE P

DATE 07 OCT 2021



GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

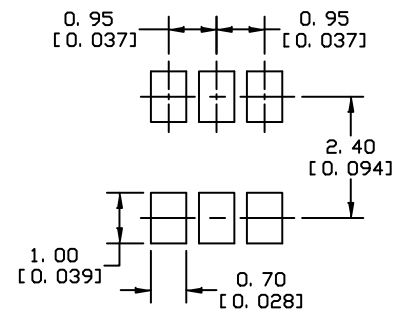
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
H _E	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0°	---	10°	0°	---	10°



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

SOLDERING FOOTPRINT

STYLE 1: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. ANODE 6. CATHODE	STYLE 2: PIN 1. NO CONNECTION 2. COLLECTOR 3. EMITTER 4. NO CONNECTION 5. COLLECTOR 6. BASE	STYLE 3: PIN 1. EMITTER 1 2. BASE 1 3. COLLECTOR 2 4. EMITTER 2 5. BASE 2 6. COLLECTOR 1	STYLE 4: PIN 1. COLLECTOR 2 2. EMITTER 1/EMITTER 2 3. COLLECTOR 1 4. EMITTER 3 5. BASE 1/BASE 2/COLLECTOR 3 6. BASE 3	STYLE 5: PIN 1. CHANNEL 1 2. ANODE 3. CHANNEL 2 4. CHANNEL 3 5. CATHODE 6. CHANNEL 4	STYLE 6: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 7: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 8: PIN 1. EMITTER 1 2. BASE 2 3. COLLECTOR 2 4. EMITTER 2 5. BASE 1 6. COLLECTOR 1	STYLE 9: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 10: PIN 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE	STYLE 11: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR	

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