

NIS1050

Protection Interface Circuit for PMICs with Integrated OVP Control

The NIS1050 is a protection IC targeted at the latest generation of PMICs from the leading mobile phone and UMPC chipset vendors. It includes a highly stable low-current LDO and a low impedance power N-Channel MOSFET.

The LDO provides a low current, five volt supply to the PMIC, and the NFET is the external pass element for the OVIC circuit. These stages combine with the internal PMIC to protect the charging circuit from low-impedance overvoltage conditions that can occur from either the AC/DC or USB supply.

The NIS1050 is available in the low-profile 6-lead 2x2mm WDFN6 surface mount package.

Features

- Lower Power Dissipation and Higher Efficiency vs. Zener Shunt Regulator
- LDO Highly Stable across Temperature, Operates Without Bypass Capacitors
- Wide 3-30 V Power Supply Voltage Input Range
- Low-Profile (0.75mm) 6-Lead 2x2mm WDFN6 Package
- This is a Pb-Free Device

Typical Applications

- Power Interface for New Generation PMICs from Leading Mobile Phone and UMPC Chipset Vendors



ON Semiconductor®

<http://onsemi.com>



WDFN6, 2x2
CASE 506AN

MARKING DIAGRAMS



PM = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NIS1050MNTBG	WDFN6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

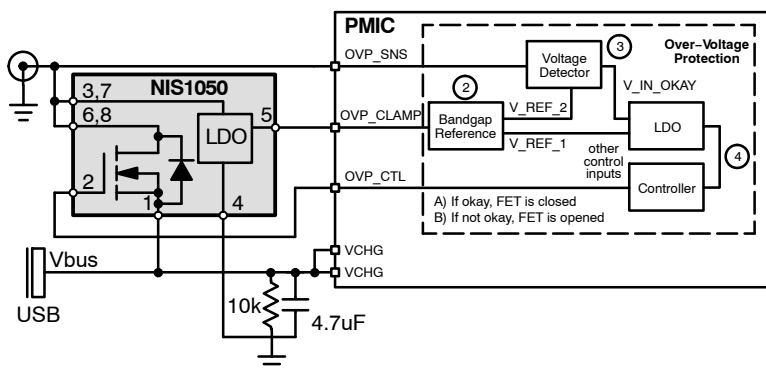


Figure 1. Typical Application

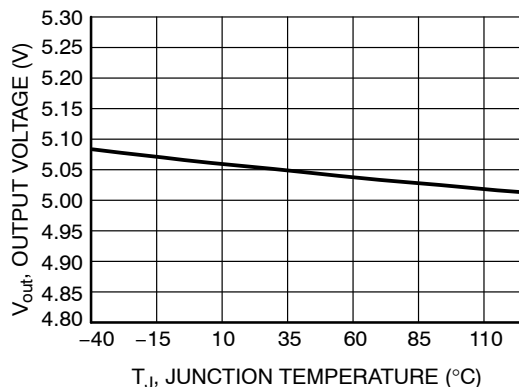


Figure 2. Output Voltage Variation with Temperature

NIS1050

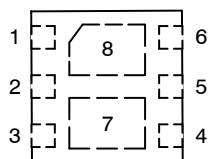


Figure 3. Pin Assignment

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Function	Description
1	Source	This is the source of the power FET and connects to the PMIC pin of the same name.
2	Gate	This pin is the gate of the FET switch.
3, 7	V _{in}	Positive input voltage to the device.
4	Ground	Negative input voltage to the device. This is used as the internal reference for the IC.
5	V _{out}	This is the output of the internal LDO. It passes the input voltage through to the output and clamps that voltage if it exceeds the regulation limit.
6, 8	Drain	Positive input voltage to the device.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, Operating, Steady-State (OVP_sense to Gnd)	V _{in}	-0.3 to 30	V
Gate-to-Source Voltage	V _{GS}	±8	V
Drain Current, Peak (10 μs pulse)	I _{Dpk}	20	A
Drain Current, Continuous (Note 1, Steady-State) T _A = 25°C T _A = 85°C	I _D	3.7 2.7	A
Total Power Dissipation @ T _A = 25°C (Note 1, 2)	P _{max}	750	mW
Operating Temperature Range	T _J	-40 to 125	°C
Non-operating Temperature Range	T _J	-55 to 150	°C
Maximum Lead Temperature for Soldering Purposes	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm², 2 oz Cu.
2. Dual die operation (equally-heated).

Table 3. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
SINGLE DIE OPERATION (SELF-HEATED)			
Junction-to-Ambient – Steady State (Note 3)	R _{θJA}	83	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	R _{θJA}	177	
Junction-to-Ambient – t ≤ 5 s (Note 3)	R _{θJA}	54	
DUAL DIE OPERATION (EQUALLY-HEATED)			
Junction-to-Ambient – Steady State (Note 3)	R _{θJA}	58	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	R _{θJA}	133	
Junction-to-Ambient – t ≤ 5 s (Note 3)	R _{θJA}	40	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

NIS1050

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} (OVP_sense) = 5.0 V, T_J = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Zero Gate Voltage Drain Current ($V_{DS} = 24 V_{dc}$, $V_{GS} = 0 V$) $T_J = 85^\circ C$	I_{DSS}			1.0 10	μA
Gate-to-Source Leakage Current ($V_{DS} = 0 V$, $V_{GS} = \pm 8 V$)	I_{GSS}			100	nA
Gate Threshold Voltage ($V_{GS} = V_{DS}$, $I_D = 250 \mu A$)	$V_{GS(th)}$	0.4	0.7	1.0	V
Negative Gate Threshold Temperature Coefficient	$V_{GS(th)}/T_J$		2.8		mV/°C
Drain-to-Source On-Resistance (Note 5) $V_{GS} = 4.5 V$, $I_D = 2.0 A$ $V_{GS} = 2.5 V$, $I_D = 2.0 A$	$R_{DS(on)}$		47 56	70 90	m Ω
Forward Transconductance ($V_{DS} = 5 V$, $I_D = 2.0 A$)	g_{FS}		4.5		S
Input Capacitance ($V_{DS} = 15 V_{dc}$, $V_{GS} = 0 V_{dc}$, $f = 1 MHz$)	C_{ISS}		427		pF
Output Capacitance ($V_{DS} = 15 V_{dc}$, $V_{GS} = 0 V_{dc}$, $f = 1 MHz$)	C_{OSS}		51		pF
Reverse Transfer Capacitance ($V_{DS} = 15 V_{dc}$, $V_{GS} = 0 V_{dc}$, $f = 1 MHz$)	C_{RSS}		32		pF
LDO (Unless otherwise noted, $T_J = 25^\circ C$, $V_{in} = 5.0 V$)					
Regulated Output Voltage ($V_{CC} = 5.5 V$ $I_o = 1 mA$)	V_{out}	4.6	5.0	5.3	V
Response to Input Transient (V_{in} 0 to 30 volts, $<1 \mu s$ rise time, 5.0 k Ω resistive load, Note 6) Time for signal above 5.5 volts Peak Voltage	t_{pulse} V_{pk}			5.0 9.0	μs V
Headroom ($V_{in} - V_{out}$, $I_{out} = 1.2 mA$, $V_{in} = 4.6 V$)	V_{head}			150	mV
Headroom ($V_{in} - V_{out}$, $I_{out} = 10 mA$, $V_{in} = 4.8 V$, $T_J = -40$ to $125^\circ C$)	V_{head}			1000	mV
TOTAL DEVICE					
Input Bias Current	I_{bias}		110	850	μA
Minimum Operating Voltage	V_{in-min}			3.0	V

5. Pulse test: Pulse width 300 μs , duty cycle 2%.

6. Guaranteed by design.

TYPICAL PERFORMANCE CURVES

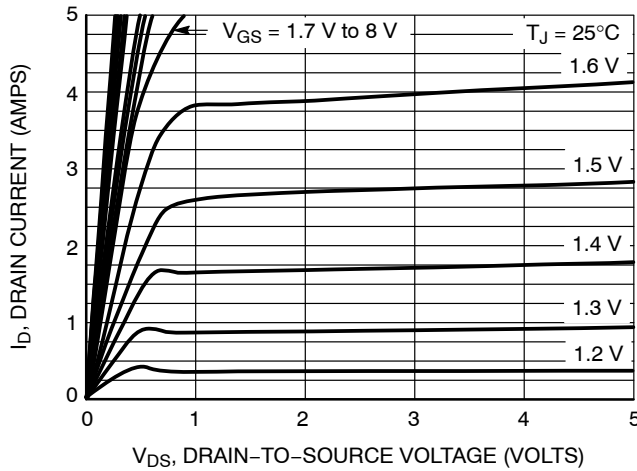


Figure 4. On-Region Characteristics

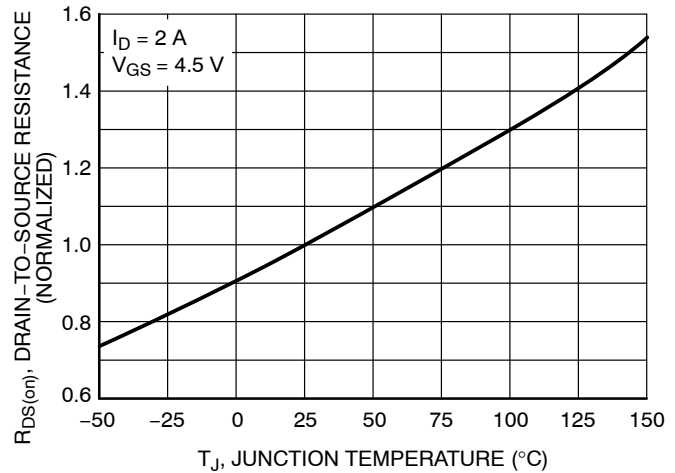


Figure 5. On-Resistance Variation with Temperature

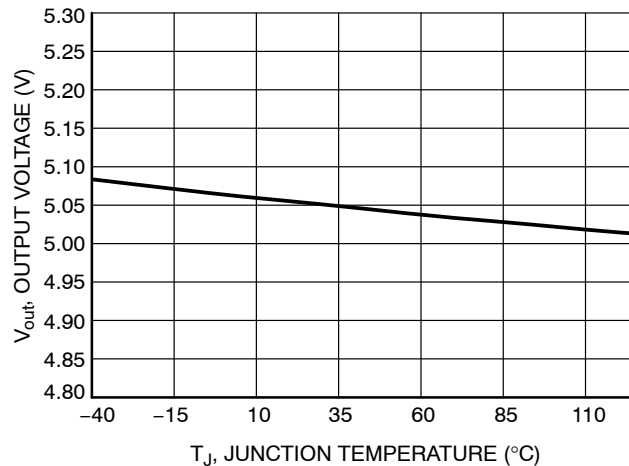


Figure 6. Output Voltage Variation with Temperature

Mounting Considerations

The LDO and MOSFET are both attached to thermal pads to provide a low impedance path for the heat generated in these devices. Both of these pads should have a solid connection to as much board copper area as possible in order to maintain a low operating temperature. The main purpose of both of these pads is for thermal connections, not electrical connections.

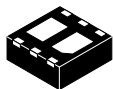
Pad 7 is the input voltage for the LDO. It is electrically connected to the Vcc pin. This connection is optional and will have a negligible difference in the electrical performance of the chip due to the current into the LDO.

Pad 8 is the drain of the power MOSFET. This pad will also have a low electrical impedance. Either pad 8, pad 6 or both may be used for electrical connections. The total

impedance of the FET will not vary significantly since pad 6 is part of the lead-frame and therefore connected to pad 8 by a metal path on the lead frame. The majority of the package impedance comes from the resistance between the source and pin 1, since this is connected by bond wires.

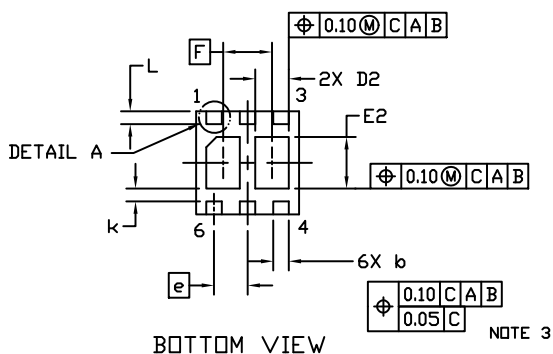
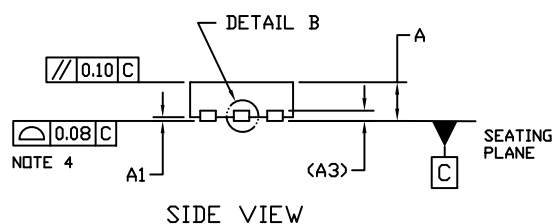
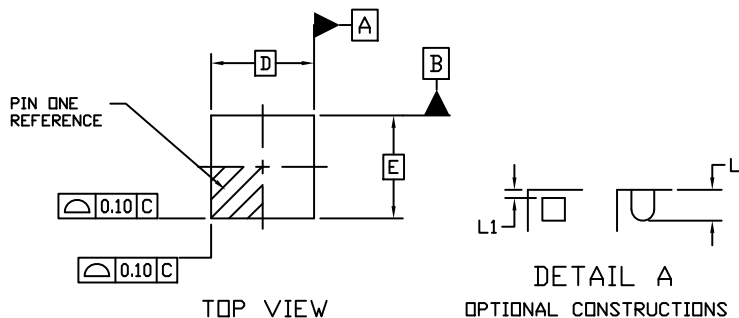
Bypass Capacitors

The LDO has been designed to operate in a stable mode without bypass capacitors; however, it is recommended to use a low ESR capacitor if fast, ac transients or other switching type currents will be present. Typically, a value of 1 to 10 nF is adequate for an output bypass capacitor. A 1 nF capacitor may be added to the input if the input source is noisy or if it has a high ac impedance due to long trace lengths.



WDFN6 2x2, 0.65P
CASE 506AN
ISSUE H

DATE 25 JAN 2022



GENERIC
MARKING DIAGRAM*



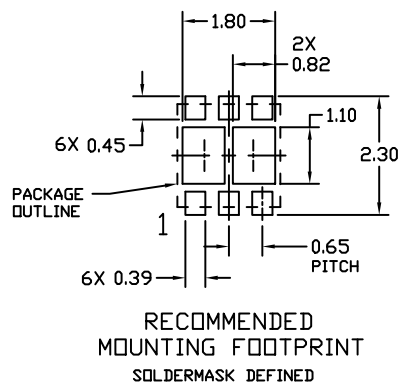
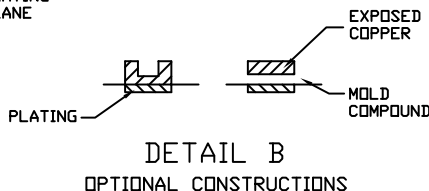
XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN.	MAX.
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.95 BSC	
k	0.25 REF	
L	0.20	0.30
L1	---	0.10



DOCUMENT NUMBER:	98AON20861D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WDFN6 2x2, 0.65P	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales