High Voltage Switcher for Offline Power Supplies

NCP1124, NCP1126, NCP1129

PDIP−7
P SUFFIX
CASE 626B

The NCP112x products integrates a fixed−frequency peak current mode controller with a low on−resistance, 650 V MOSFET. Available in a PDIP−7 package, the NCP112x offers a high level of integration, including soft−start, frequency−jittering, short−circuit protection, thermal shutdown protection, frequency foldback mode and skip−cycle to reduce power consumption in light load condition, peak current mode control with adjustable internal ramp compensation and adjustable peak current set point.

During nominal load operation, the part switches at one of the available frequencies (65 or 100 kHz). When the output power demand diminishes, the IC automatically enters frequency foldback mode and provides excellent efficiency at light loads. When the power demand reduces further, it enters into a skip mode to reduce the standby consumption down to no load condition.

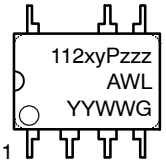
Protection features include: a timer to detect an overload or a short−circuit event with auto−recovery or latch protection, and a built−in V_{CC} overvoltage protection.

The switcher also provides a jittered 65 kHz or 100 kHz switching frequency to improve the EMI.

Features

- Built−in 650 V, 1 A MOSFET with $R_{DS(on)}$ of 8.6 Ω for NCP1124
- Built−in 650 V, 1.8 A MOSFET with $R_{DS(on)}$ of 5.4 Ω for NCP1126
- Built−in 650 V, 5.5 A MOSFET with $R_{DS(on)}$ of 2.1 Ω for NCP1129
- Fixed−Frequency 65 or 100 kHz Current Mode Control with Adjustable Internal Ramp Compensation
- Adjustable Current Limit with External Resistor
- Frequency Foldback Down to 26 kHz and Skip−Cycle for Light Load Efficiency
- Frequency Jittering for EMI Improvement
- Less than 100 mW Standby Power @ High Line
- EPS 2.0 Compliant
- 7−Pin Package Provides Creepage Distance
- These are Pb−Free Devices

MARKING DIAGRAMS



x	= Specific Device Code 4 = NCP1124 6 = NCP1126 9 = NCP1129
y	= A or B A = Latch B = Auto−recovery
zzz	= Frequency 65 = 65 kHz 100 = 100 kHz
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

Table 1. OUTPUT POWER TABLE (Note 1)

Product	230 Vac ± 15% (Note 4)		85 – 265 Vac	
	Adapter (Note 2)	**Peak or Open Frame** (Note 3)	**Adapter** (Note 2)	**Peak or Open Frame** (Note 3)
NCP1124	12 W	27 W	6 W	14 W
NCP1126	15 W	32 W	10 W	17 W
NCP1129	28 W	43 W	20 W	26.5 W

1. 12 V output voltage with 135 V reflected output voltage
2. Typical continuous power in a non-ventilated enclosed adaptor measured at 50°C ambient temperature.
3. Maximum practical continuous power in an open-frame design at 50°C ambient temperature
4. 230 V_{AC} or 115 V_{AC} with voltage doubler.

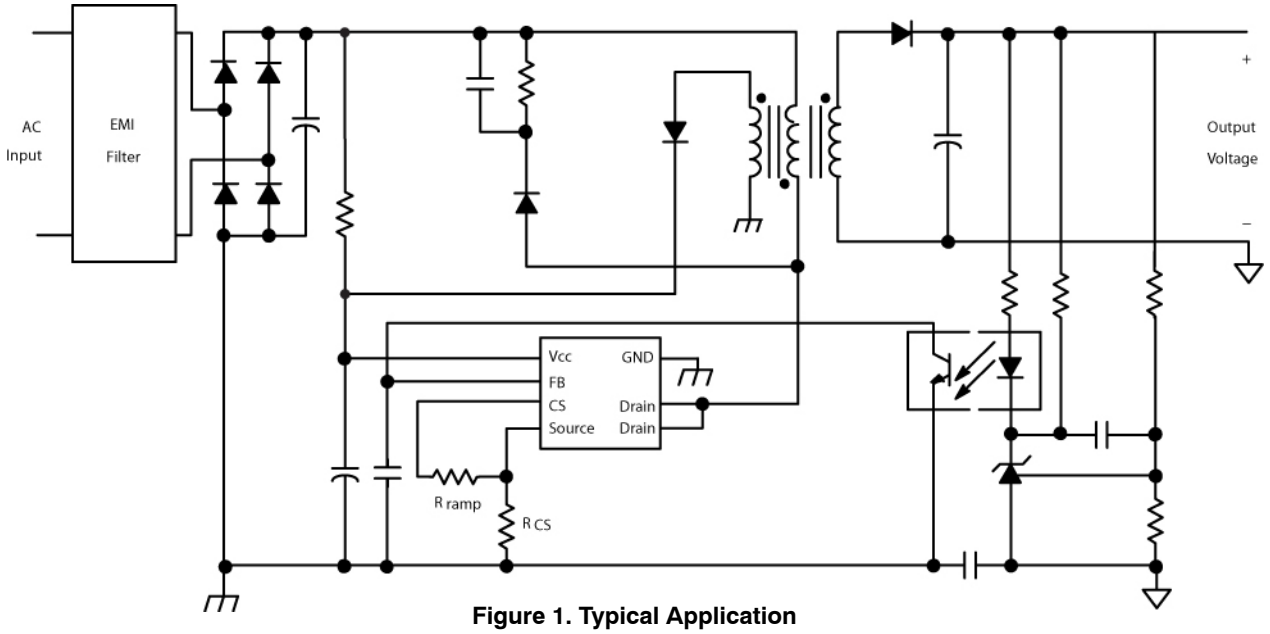


Figure 1. Typical Application

Table 2. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Description
1	VCC	This pin is connected to an external auxiliary voltage and supplies the controller. When above a certain level, the part fully latches off.
2	FB	Feedback input. Hooking an optocoupler collector to this pin will allow regulation.
3	CS	This pin monitors the primary peak current but also offers a means to introduce ramp compensation.
4	Source	Source of the internal MOSFET. This pin is typically connected to the source of a grounded sense resistor.
5	Drain	The drain of the internal MOSFET. These pins connect to the transformer terminal and can withstand up to 650 V.
6	Drain	
7	–	Removed for creepage distance.
8	GND	Ground reference.

Table 3. OPTIONS

Switcher	Package	Frequency	Short−Circuit Protection
NCP1124AP65G	PDIP−7	65 kHz	Latch
NCP1124BP65G	PDIP−7	65 kHz	Auto−Recovery
NCP1124AP100G	PDIP−7	100 kHz	Latch
NCP1124BP100G	PDIP−7	100 kHz	Auto−Recovery
NCP1126AP65G	PDIP−7	65 kHz	Latch
NCP1126BP65G	PDIP−7	65 kHz	Auto−Recovery
NCP1126AP100G	PDIP−7	100 kHz	Latch
NCP1126BP100G	PDIP−7	100 kHz	Auto−Recovery
NCP1129AP65G	PDIP−7	65 kHz	Latch
NCP1129BP65G	PDIP−7	65 kHz	Auto−Recovery
NCP1129AP100G	PDIP−7	100 kHz	Latch
NCP1129BP100G	PDIP−7	100 kHz	Auto−Recovery

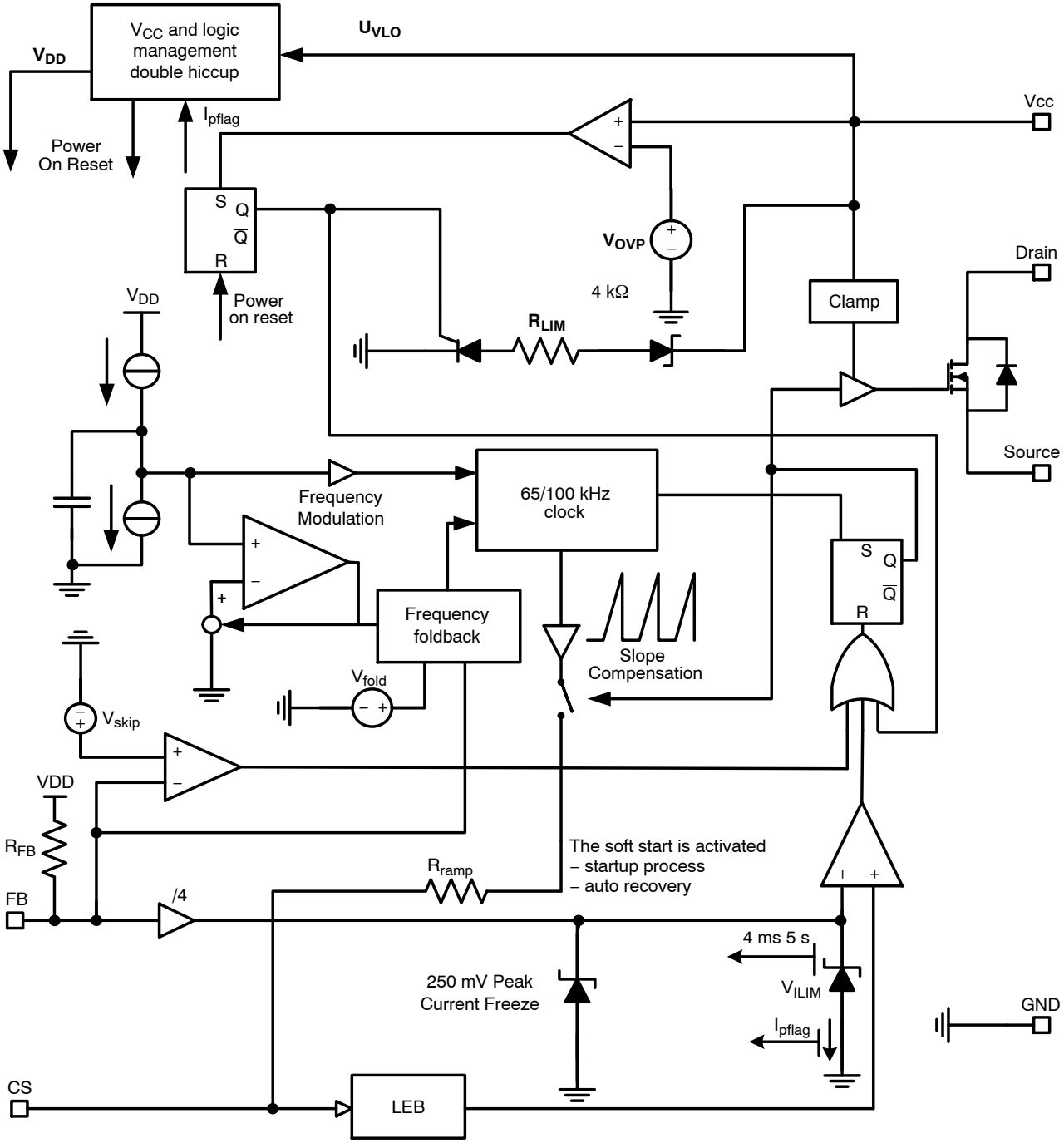


Figure 2. Functional Block Diagram

Table 4. MAXIMUM RATINGS (Note 5)

Rating		Symbol	Value	Unit
Drain Input Voltage (Referenced to Source Terminal)	NCP112x	V_{Drain}	−0.3 to 650	V
Drain Maximum Pulsed Current (10 μs Single Pulse, T_J = 25°C)	NCP1129 NCP1126 NCP1124	I_{DM}	27 11 7	A
Single Pulse Avalanche Energy	NCP1126, NCP1129 NCP1124	E_{AS}	96 60	mJ
Supply Input Voltage		$V_{CC(MAX)}$	−0.3 to 35	V
Current Sense Input Voltage		V_{CS}	−0.3 to 10	V
Feedback Input Voltage		V_{FB}	−0.3 to 10	V
Operating Junction Temperature		T_J	−40 to 150	°C
Storage Temperature Range		T_{STG}	−60 to 150	°C
Power Dissipation (T_A = 25°C, 2 Oz Cu, 600 mm^2 Printed Circuit Copper Clad)		P_D	1.5	W
Thermal Resistance, Junction to Ambient 2 Oz Cu Printed Circuit Copper Clad Low Conductivity (Note 6) High Conductivity (Note 7)		$R_{\theta JA}$	 128 78	°C/W
ESD Capability (Note 8) Human Body Model ESD Capability per JEDEC JESD22−A114F. Machine Model ESD Capability per JEDEC JESD22−A115C. Charged−Device Model ESD Capability per JEDEC JESD22−C101E.			 2000 200 500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5. This device contains Latch−Up protection and exceeds ±100 mA per JEDEC Standard JESD78.
6. Low Conductivity Board. As mounted on 40 x 40 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper trances and heat spreading area. As specified for a JEDEC 51 low conductivity test PCB. Test conditions were under natural convection of zero air flow.
7. High Conductivity Board. As mounted on 40 x 40 x 1.5 mm FR4 substrate with a single layer of 600 mm^2 of 2 oz copper trances and heat spreading area. As specified for a JEDEC 51 high conductivity test PCB. Test conditions were under natural convection of zero air flow.
8. The Drain pins (5 and 6), are rated to the maximum voltage of the device, or 650 V.

Table 5. ELECTRICAL CHARACTERISTICS
(V_{CC} = 12 V, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	15.75	17	20	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	7.75	8.5	9.25	
Operating Hysteresis	$V_{CC(on)} - V_{CC(off)}$	$V_{CC(HYS)}$	6.0	–	–	
V_{CC} Overvoltage Protection Threshold		$V_{CC(OVP)}$	26.3	28	29.3	V
V_{CC} Overvoltage Protection Filter Delay		$t_{OVP(delay)}$	–	26	–	μs
V_{CC} Clamp Voltage in Latch Mode	I_{CC} = 500 μA	V_{ZENER}	5	6.2	7.15	V
Supply Current						μA
Startup Current	$V_{CC} = V_{CC(on)} - 0.5$ V	I_{CC1}	–	–	15	
Skip Current	$V_{FB} = V_{skip} - 0.1$ V	I_{CC2}	–	700	900	
Operating Current at 65 kHz	I_{FB} = 50 μA, f_{SW} = 65 kHz	I_{CC3}	–	1900	3100	
Operating Current at 100 kHz	I_{FB} = 50 μA, f_{SW} = 100 kHz	I_{CC4}	–	3300	4000	
Current Consumption in Latch Mode	T_J = −40°C to 125°C	$I_{CC(latch)}$	42	–	–	μA
POWER SWITCH CIRCUIT						
Off−State Leakage Current	T_J = 125°C, V_{Drain} = 650 V	$I_{Drain(off)}$	–	–	20	μA
Breakdown Voltage	T_J = 25°C, I_{Drain} = 250 μA, V_{FB} = 0 V	$V_{BR(DSS)}$	650	–	–	V
ON State Resistance	I_{Drain} = 100 mA	$R_{DS(on)}$				Ω
NCP1129	V_{CC} = 10 V, T_J = 25°C		–	2.1	2.75	
	V_{CC} = 10 V, T_J = 125°C		–	–	5.0	
NCP1126	V_{CC} = 10 V, T_J = 25°C		–	5.4	7.7	
	V_{CC} = 10 V, T_J = 125°C		–	–	13.1	
NCP1124	V_{CC} = 10 V, T_J = 25°C		–	9.0	13.2	
	V_{CC} = 10 V, T_J = 125°C		–	–	23.5	
Output Capacitance NCP1129	V_{DS} = 25 V, V_{CC} = 0 V, f = 1 MHz	C_{OSS}	–	67.3	–	pF
NCP1126	V_{DS} = 25 V, V_{CC} = 0 V, f = 1 MHz		–	29.2	–	
NCP1124	V_{DS} = 25 V, V_{CC} = 0 V, f = 1 MHz		–	16.5	–	
Switching Characteristics						ns
NCP1124 Rise Time	(V_{DS} = 325 V, I_{Drain} = 1 A,	t_r	–	4.25	–	
Fall Time	V_{GS} = 10 V, R_g = 4.7 Ω)	t_f	–	9.32	–	
NCP1126 Rise Time	(V_{DS} = 325 V, I_{Drain} = 1.8 A,	t_r	–	7.44	–	
Fall Time	V_{GS} = 10 V, R_g = 4.7 Ω)	t_f	–	5.94	–	
NCP1129 Rise Time	(V_{DS} = 325 V, I_{Drain} = 5.5 A,	t_r	–	7.54	–	
Fall Time	V_{GS} = 10 V, R_g = 4.7 Ω)	t_f	–	5.94	–	
CURRENT SENSE						
Current Sense Voltage Threshold	V_{CS} increasing, T_J = 25°C	V_{ILIM1}	730	785	840	mV
	V_{CS} increasing	V_{ILIM2}	720	800	880	
Cycle by Cycle Current Sense Propagation Delay	V_{CS} dv/dt = 1 V/μs, measured from V_{ILIM1} to DRV falling edge	$t_{CS(delay)}$				ns
NCP1129			–	100	150	
NCP1126			–	50	150	
NCP1124			–	50	150	
Cycle by Cycle Leading Edge Blanking Duration		$t_{CS(LEB)}$	–	320	400	ns
INTERNAL OSCILLATOR						
Oscillation Frequency	65 kHz Version	f_{OSC1}	61	65	71	kHz
	100 kHz Version	f_{OSC2}	92	100	108	
Maximum Duty Ratio		D_{MAX}	78	80	82	%
Frequency Jittering in Percentage of f_{OSC}		f_{jitter}	–	±5	–	%

Table 5. ELECTRICAL CHARACTERISTICS
(V_{CC} = 12 V, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
FEEDBACK SECTION						
Internal Pull−up Resistor		R_{up}	–	13	–	kΩ
Equivalent ac resistor from FB to GND		R_{eq}	–	15	–	kΩ
V_{FB} to Internal Current Setpoint Division Ratio		I_{ratio}	–	4	–	–
Feedback Voltage Below Which the Peak Current is Frozen		$V_{FB(freeze)}$	0.85	1	1.15	V
FREQUENCY FOLDBACK						
Frequency Foldback Level on the FB	47% of maximum peak current	$V_{FB(fold)}$	1.35	1.5	1.78	V
Transition Frequency Below Which Skip−Cycle occurs		f_{trans}	22	26	30	kHz
Feedback voltage level when Frequency Foldback ends	$f_{SW} = f_{MIN}$	$V_{FB(fold,end)}$	410	450	490	mV
Skip−Cycle Level Voltage on The FB pin		V_{skip}	360	400	440	mV
Hysteresis on The Skip Comparator		$V_{skip(HYS)}$	–	40	–	mV
FAULT PROTECTION						
Soft−Start Period	Measured from 1st drive pulse to $V_{CS} = V_{ILIM}$	t_{SSTART}	–	4.0	–	ms
Overload Fault Timer	$V_{CS} = V_{ILIM}$	t_{OVLD}	35	50	65	ms
TEMPERATURE MANAGEMENT						
Temperature Shutdown	(Note 9)	TSD	130	–	–	°C
Hysteresis	Guaranteed by Design		–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. The value is not subjected to production test − verified by design/characterization. The thermal shutdown temperature refers to the junction temperature of the controller.

TYPICAL CHARACTERISTICS

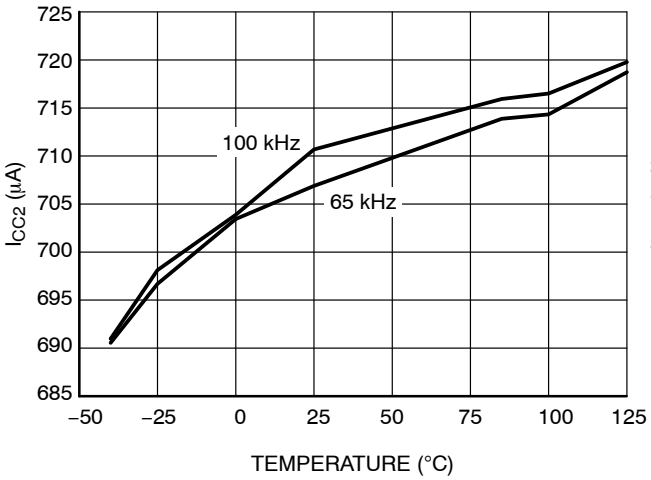


Figure 3. NCP1124 I_{CC2} vs. Junction Temperature

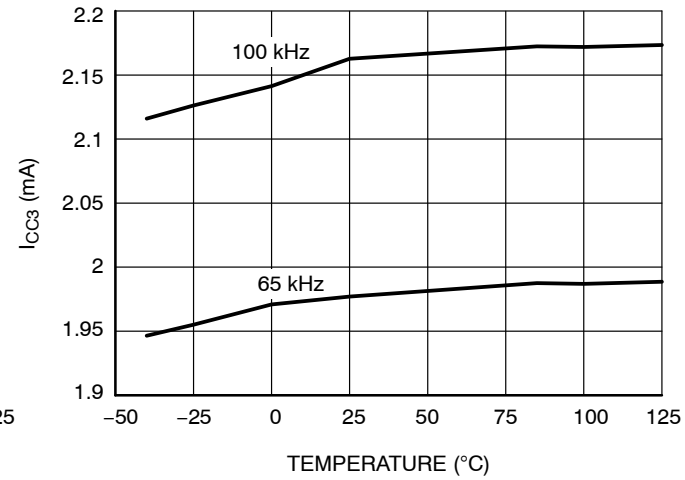


Figure 4. NCP1124 I_{CC3} vs. Junction Temperature

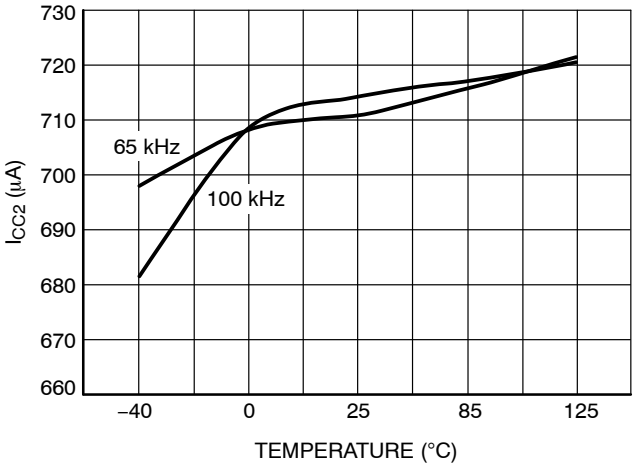


Figure 5. NCP1126 I_{CC2} vs. Junction Temperature

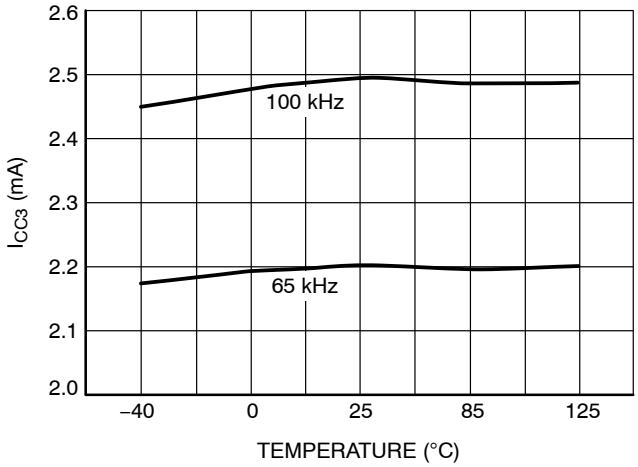


Figure 6. NCP1126 I_{CC3} vs. Junction Temperature

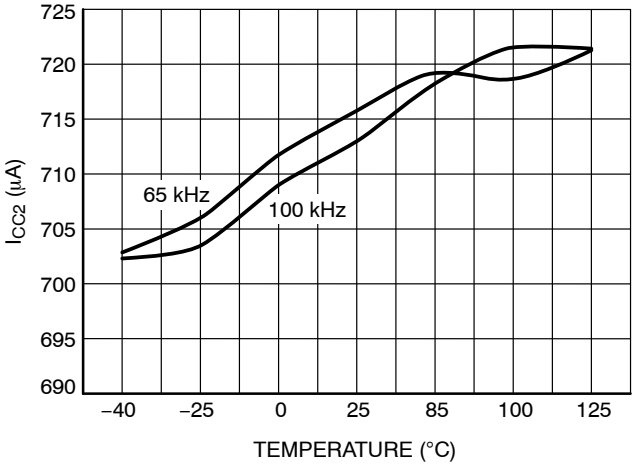


Figure 7. NCP1129 I_{CC2} vs. Junction Temperature

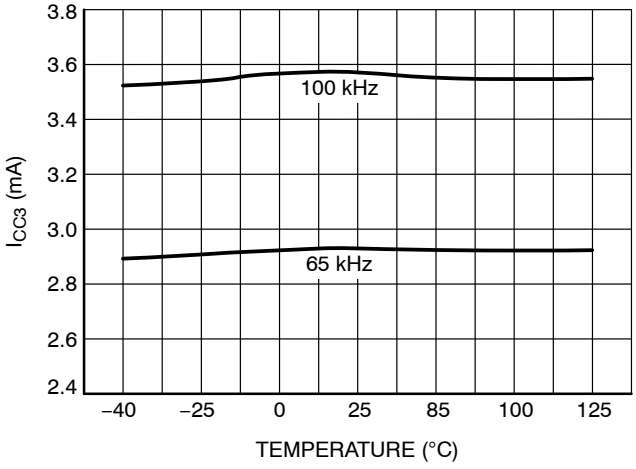


Figure 8. NCP1129 I_{CC3} vs. Junction Temperature

TYPICAL CHARACTERISTICS

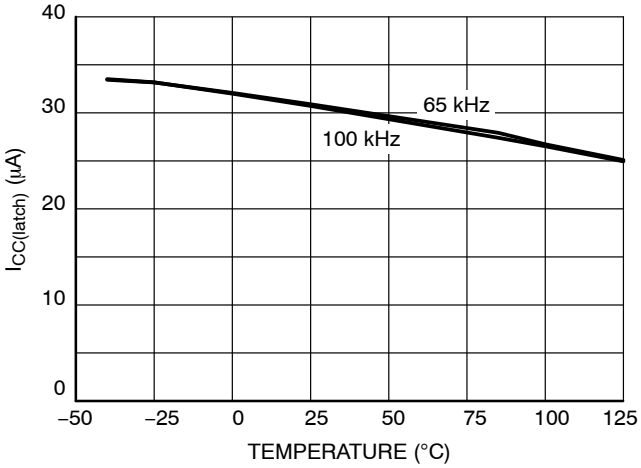


Figure 9. NCP1124 $I_{CC(latch)}$ vs. Junction Temperature

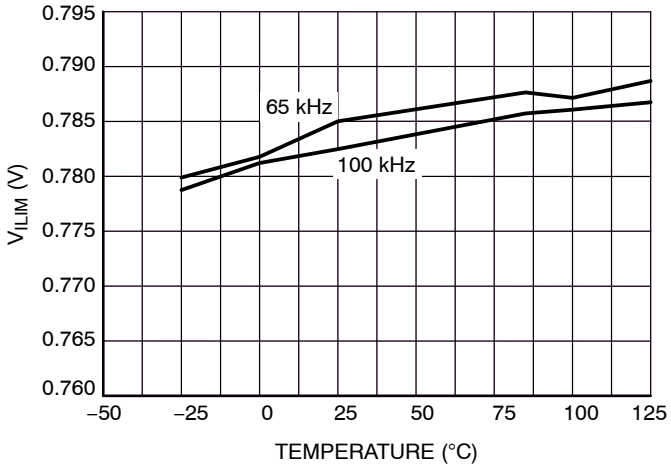


Figure 10. NCP1124 V_{ILIM} vs. Junction Temperature

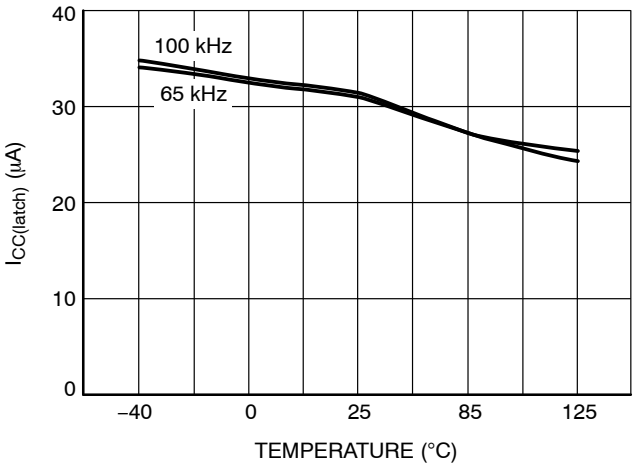


Figure 11. NCP1126 $I_{CC(latch)}$ vs. Junction Temperature

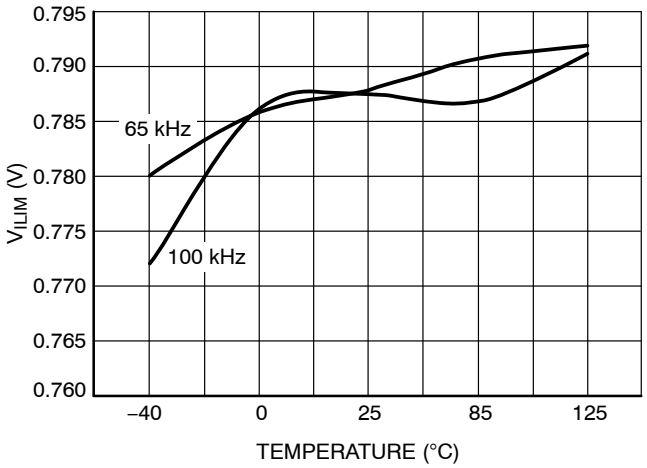


Figure 12. NCP1126 V_{ILIM} vs. Junction Temperature

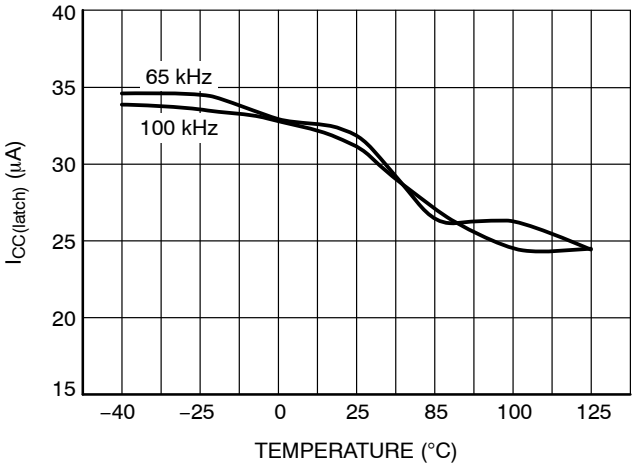


Figure 13. NCP1129 $I_{CC(latch)}$ vs. Junction Temperature

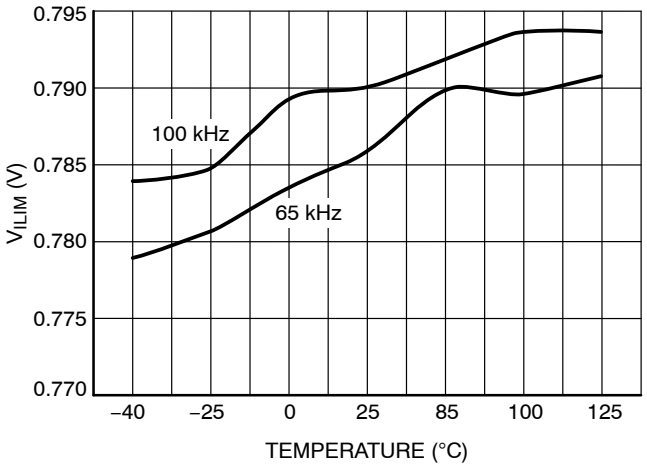


Figure 14. NCP1129 V_{ILIM} vs. Junction Temperature

TYPICAL CHARACTERISTICS

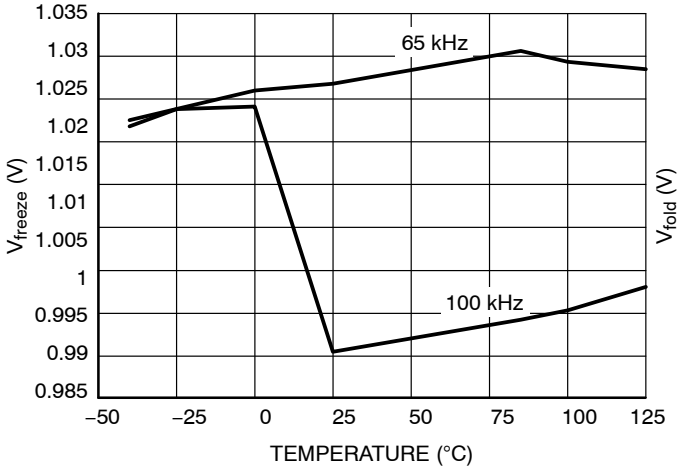


Figure 15. NCP1124 V_{freeze} vs. Junction Temperature

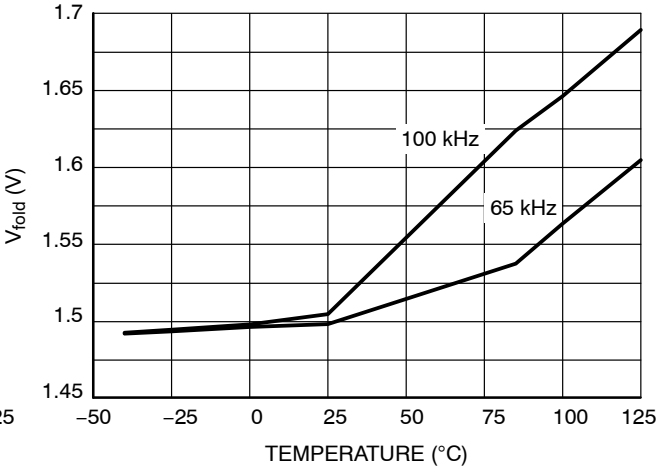


Figure 16. NCP1124 V_{fold} vs. Junction Temperature

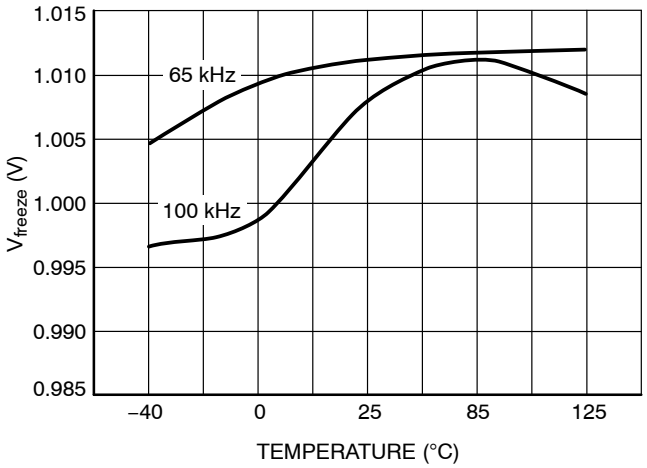


Figure 17. NCP1126 V_{freeze} vs. Junction Temperature

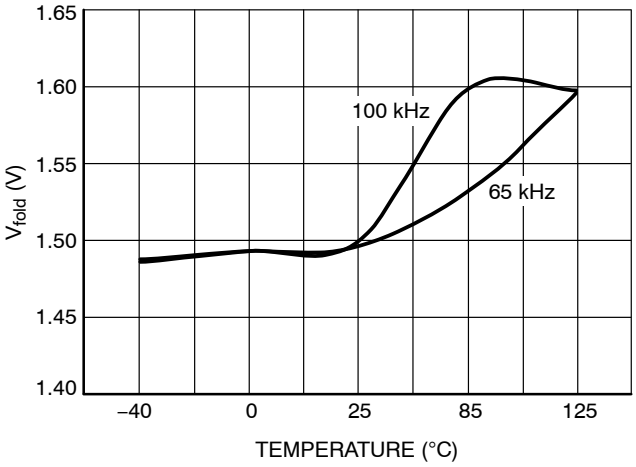


Figure 18. NCP1126 V_{fold} vs. Junction Temperature

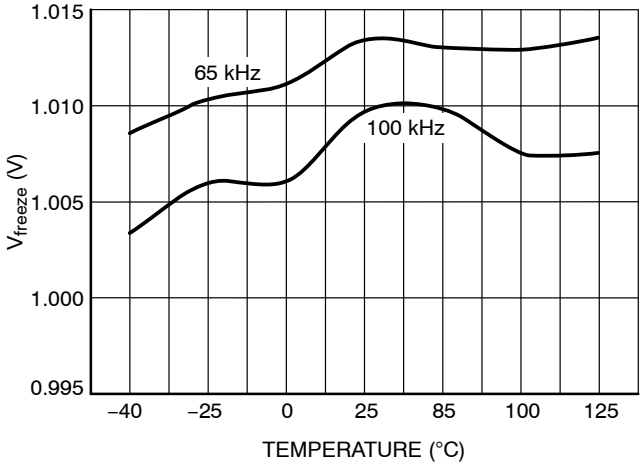


Figure 19. NCP1129 V_{freeze} vs. Junction Temperature

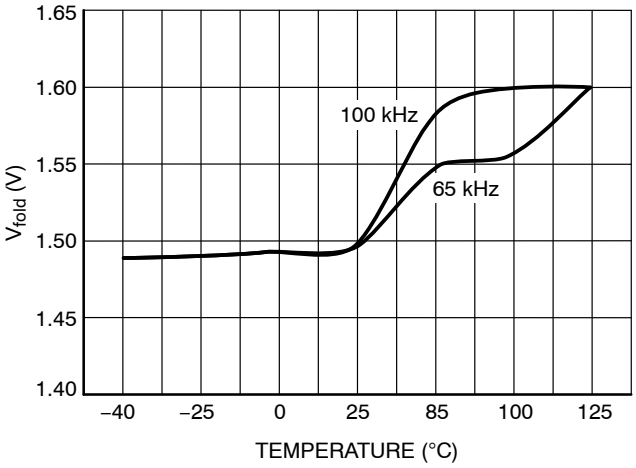


Figure 20. NCP1129 V_{fold} vs. Junction Temperature

TYPICAL CHARACTERISTICS

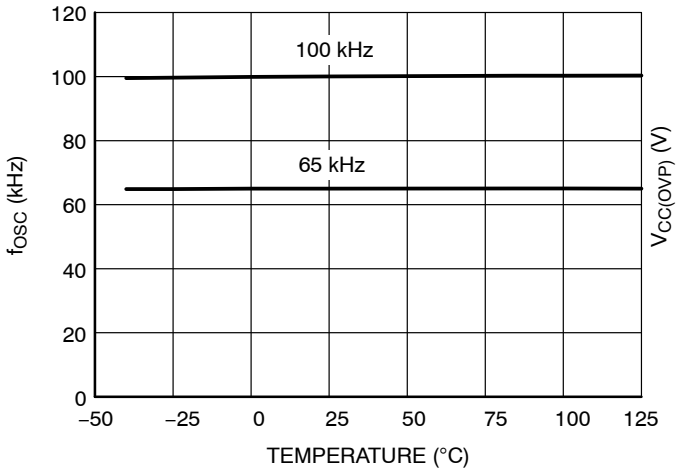


Figure 21. NCP1124 f_{OSC} vs. Junction Temperature

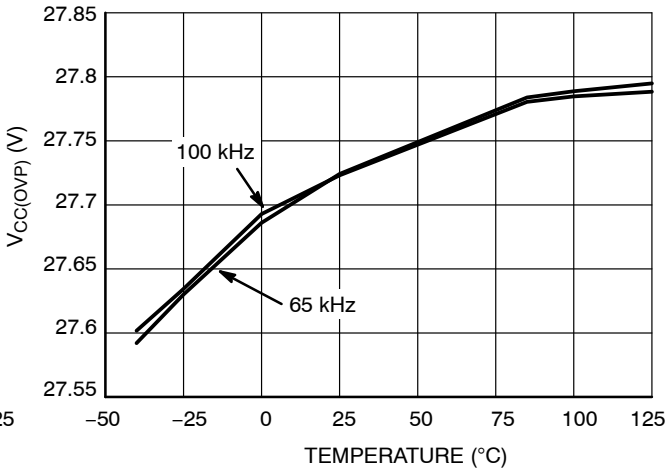


Figure 22. NCP1124 $V_{CC(OVP)}$ vs. Junction Temperature

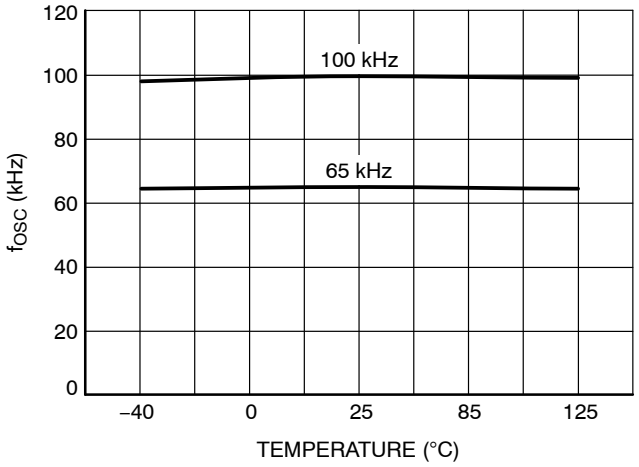


Figure 23. NCP1126 f_{OSC} vs. Junction Temperature

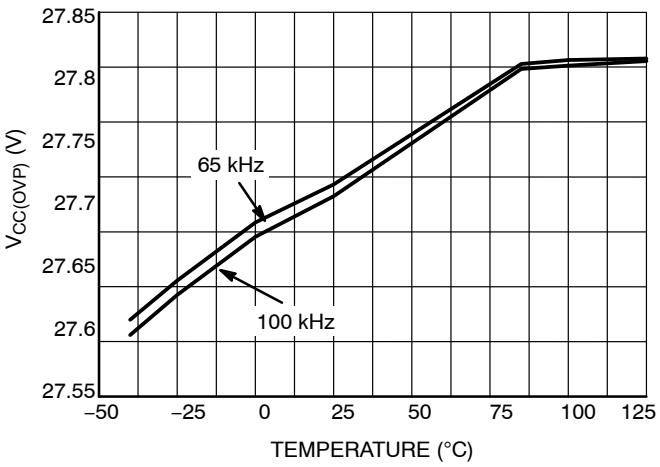


Figure 24. NCP1126 $V_{CC(OVP)}$ vs. Junction Temperature

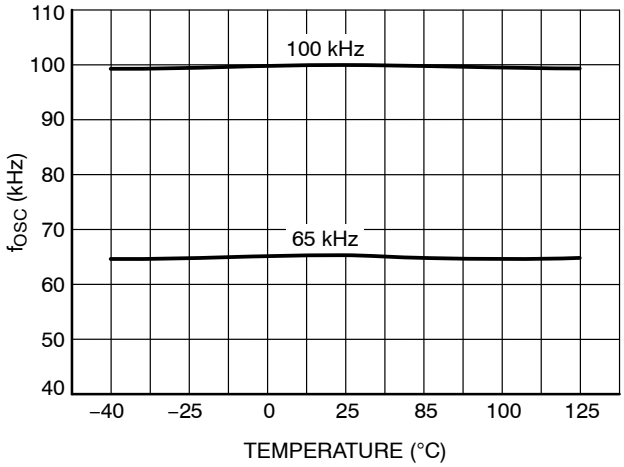


Figure 25. NCP1129 f_{OSC} vs. Junction Temperature

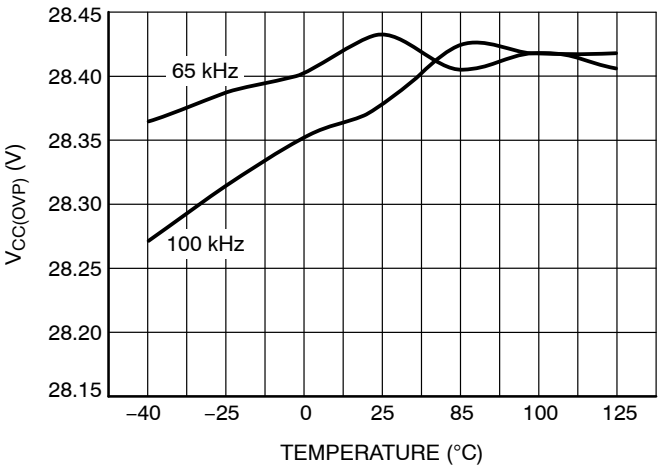


Figure 26. NCP1129 $V_{CC(OVP)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

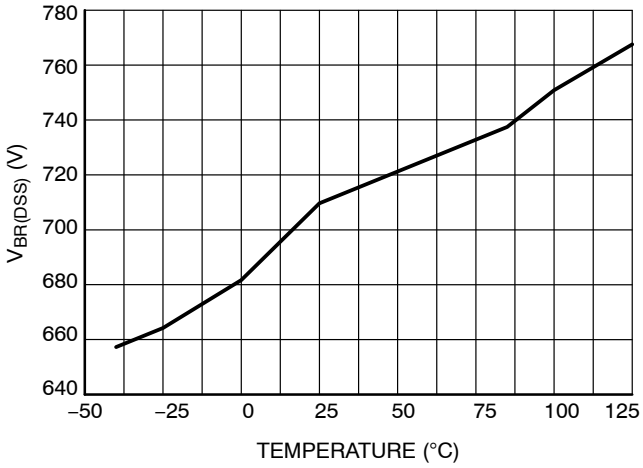


Figure 27. NCP1124 $V_{BR(DSS)}$ vs. Junction Temperature

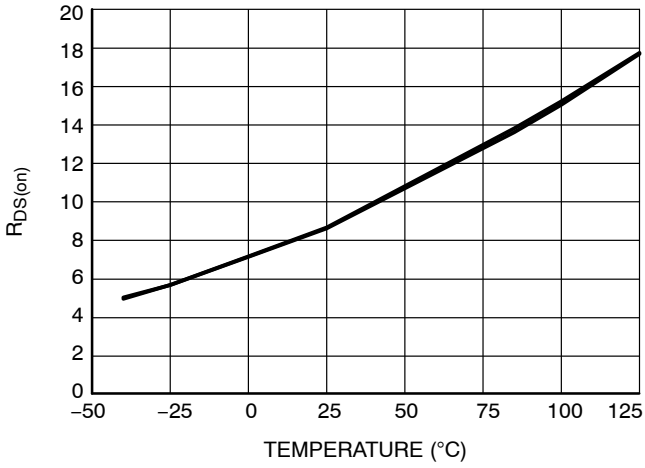


Figure 28. NCP 1124 $R_{DS(on)}$ vs. Junction Temperature

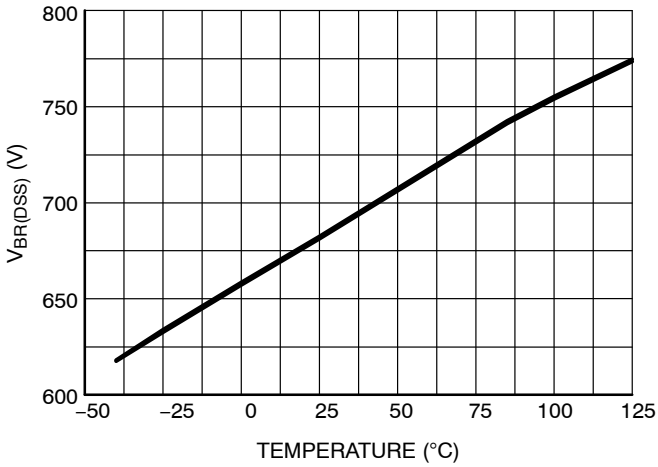


Figure 29. NCP1126 $V_{BR(DSS)}$ vs. Junction Temperature

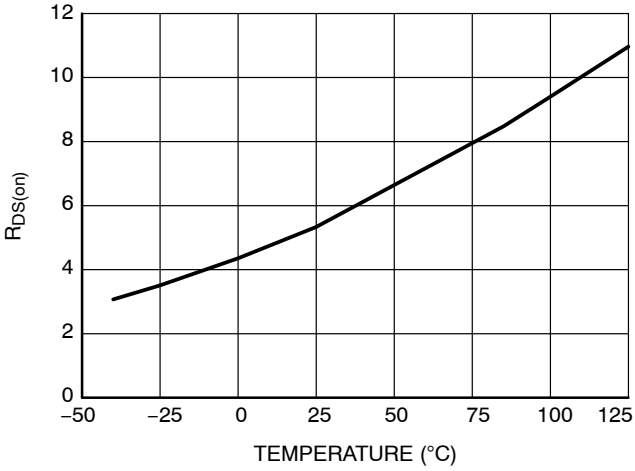


Figure 30. NCP 1126 $R_{DS(on)}$ vs. Junction Temperature

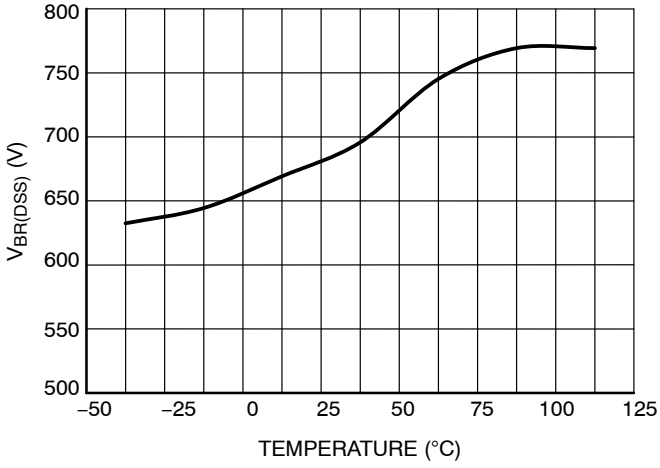


Figure 31. NCP1129 $V_{BR(DSS)}$ vs. Junction Temperature

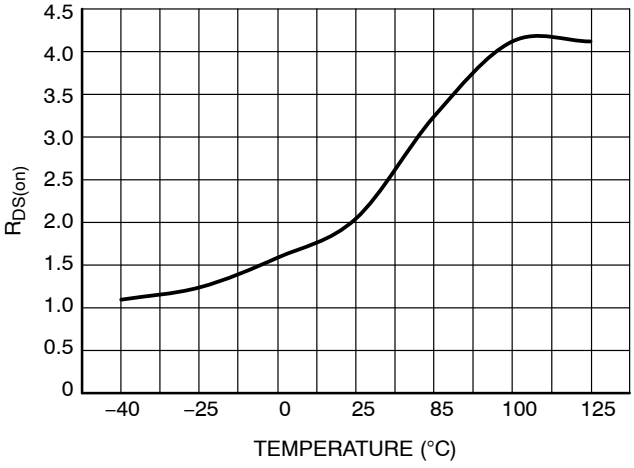


Figure 32. NCP 1129 $R_{DS(on)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

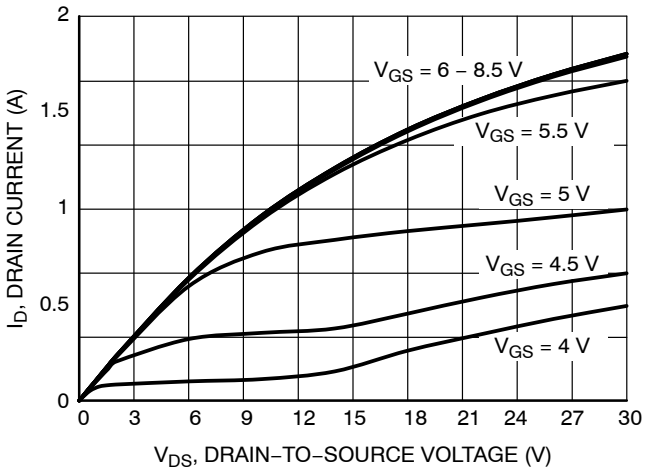


Figure 33. NCP1124 – Drain Current vs. Drain–to–Source Voltage

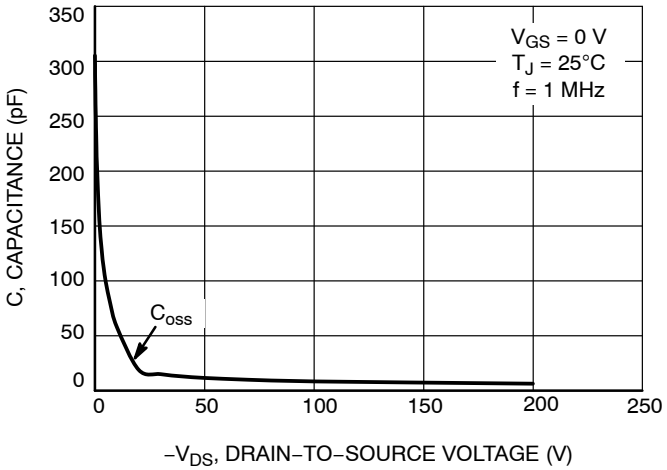


Figure 34. NCP1124 – Capacitance Variation

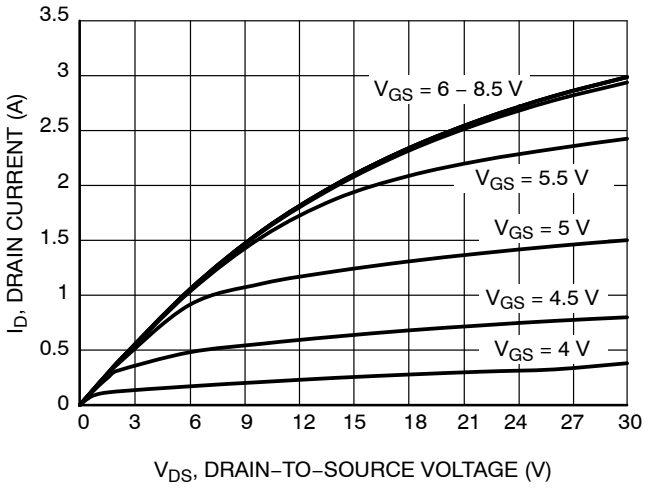


Figure 35. NCP1126 – Drain Current vs. Drain–to–Source Voltage

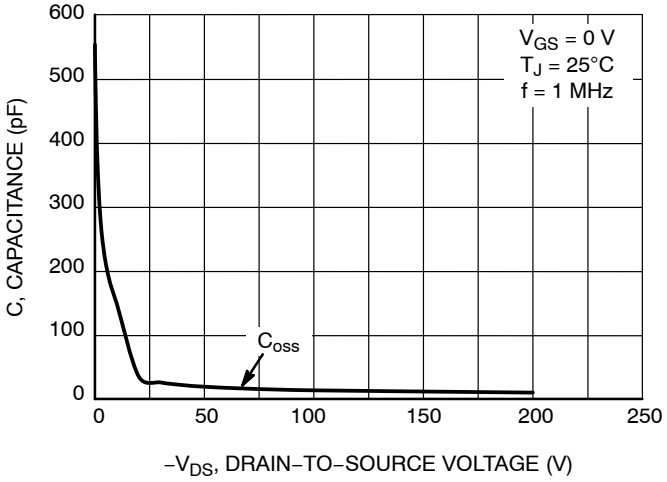


Figure 36. NCP1126 – Capacitance Variation

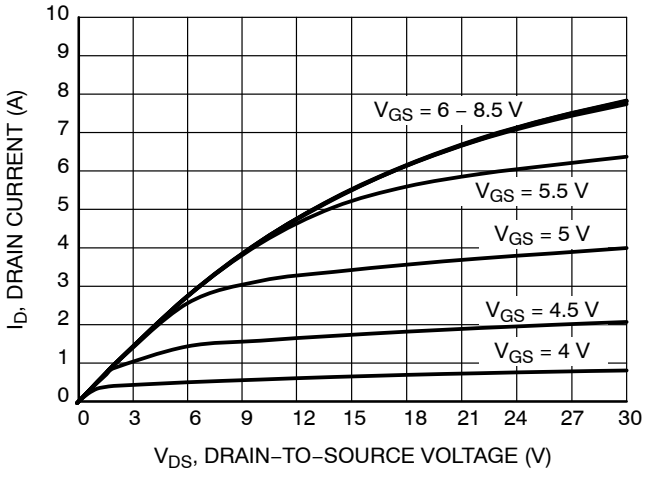


Figure 37. NCP1129 – Drain Current vs. Drain–to–Source Voltage

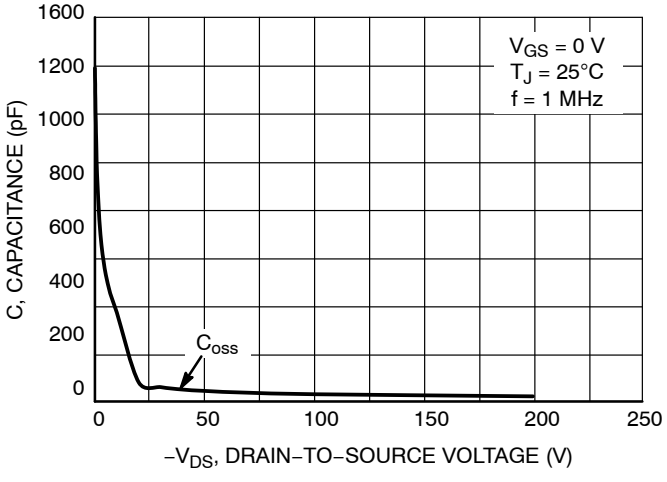


Figure 38. NCP1129 – Capacitance Variation

APPLICATION INFORMATION

Introduction

The NCP112x family integrates a high−performance current−mode controller with a 650 V MOSFET, which considerably simplifies the design of a compact and reliable switch mode power supply (SMPS). This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters. The NCP112x brings most necessary functions needed in today's modern power supply designs, with several enhancements such as V_{CC} OVP, adjustable slope compensation, frequency jittering, frequency foldback, skip cycle, etc.

- **Current−mode operation with adjustable internal ramp compensation:** Sub−harmonic oscillations in peak current mode control can be eliminated by the adjustable internal ramp compensation when the duty ratio is larger than 0.5.
- **Frequency foldback capability:** When the load current drops, the controller responds by reducing the primary peak current. When the peak current reaches the skip peak current level, the NCP112x enter skip operation to reduce the power consumption.
- **Internal soft−start:** a soft−start precludes the main power switch from being stressed upon start−up. In this switcher, the soft−start is internally fixed to 4 ms. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup.
- **Latched OVP on V_{CC}:** When the V_{CC} exceeds 28 V typical, the drive signal is disabled and the part latches off. When the user cycles the V_{CC} down, the circuit is reset and the part enters a new start up sequence.
- **Short−circuit protection:** short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between the auxiliary and the power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Every time the internal 0.8 V maximum peak current limit is activated, an error flag is asserted and an internal timer starts. When the fault is validated, the switcher will either be latched or enter the auto−recovery mode. As soon as the fault disappears, the SMPS resumes operation.
- **EMI jittering:** an internal low−frequency 240 Hz modulation signal varies the pace at which the oscillator frequency is modulated. This helps spread out the energy in a conducted noise analysis. To improve the EMI signature at low power levels, the jittering will not be disabled in frequency foldback mode (light load conditions).

Start−up Sequence

The NCP112x need an external startup circuit to provide the initial energy to the switcher. As is shown in Figure 39, the startup circuit consists of R_{start} and V_{CC} capacitor C_{CC}, connected to the main input, i.e. half−wave connection. The auxiliary winding will take over the RC circuit after the output voltage is built up.

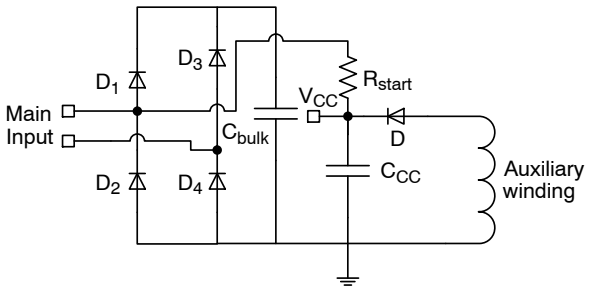


Figure 39. Startup Circuit for NCP112x (half−wave connection)

The startup process can be well explained by Figure 40. At power on, when the V_{CC} capacitor is fully discharged, the switcher current consumption is zero and does not deliver any driving pulses. The V_{CC} capacitor C_{CC} is going to be charged by the main input via R_{start}. As V_{CC} increases, the switcher consumed current remains below a guaranteed limit until the voltage on the capacitor reaches $V_{CC(on)}$, at which point the switcher starts to deliver pulses to the power MOSFET. The switcher current consumption suddenly increases, and the capacitor depletes since it is the only energy reservoir. Its voltage falls until the auxiliary winding takes over and supply the V_{CC} pin.

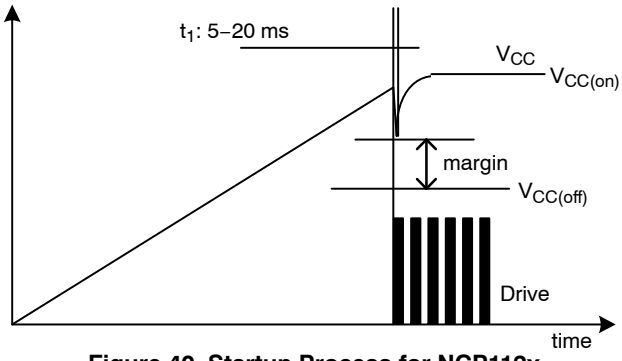


Figure 40. Startup Process for NCP112x

The start−up current of the switcher is extremely low, below 15 μA. The start−up resistor can be connected to the bulk capacitor or directly the mains input voltage for further power dissipation reduction. The switcher begins switching when V_{CC} reaches $V_{CC(on)}$, typically 17 V for NCP1126/9. From Figure 41, it can be seen that the startup resistor R_{start} and V_{CC} capacitor are about to be determined.

V_{CC} Capacitor

The supply capacitor, C_{CC}, provides power to the switcher during power up. The capacitor must be large enough such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is building up. Otherwise, V_{CC} will collapse and the switcher will turn off. Assuming this time t_1 is equal to 10 ms, Equation 1 is used to calculate the required V_{CC} capacitor.

$$C_{CC} \geq \frac{I_{CC} t_1}{V_{CC(on)} - V_{CC(off)}} \quad \text{(eq. 1)}$$

Startup Resistor R_{start}

In order to determine the startup resistor, the V_{CC} capacitor charging current is calculated first to ensure that the charging time for the V_{CC} capacitor from 0 V to its operating voltage meets the startup time requirement. Equation 2 gives the first constraints for the R_{start} selection.

$$I_{charge} \geq \frac{V_{CC(on)} C_{CC}}{t_{startup}} \quad \text{(eq. 2)}$$

For NCP1126/9, during startup process, from 0 to t_1, the current that flow inside the switcher is I_{CC1}, therefore the total charging current from the main input is going to be $I_C = I_{charge} + I_{CC1}$. Consider the half−wave connection start−up network to the mains as is shown in Figure 41, the average current flowing into this start−up resistor will be the smallest when V_{CC} reaches the $V_{CC(on)}$ of the switcher:

$$I_{c,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{R_{start-up}} \quad \text{(eq. 3)}$$

which gives the minimum value for the $R_{startup}$,

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{I_{c,min}} \quad \text{(eq. 4)}$$

Note that this calculation is purely theoretical, considering a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the V_{CC} capacitor. This brings a decrease in the charging current and an increase of the start−up resistor, for the benefit of standby power. The dissipated power at high line amounts to:

$$P_{diss} = \frac{V^2_{ac,peak}}{4R_{start}} \quad \text{(eq. 5)}$$

The above derivation is based on the case when the power supply is not at light load. V_{CC} capacitor selection should ensure that does not disappear in no−load conditions. In light load condition, the skip−cycle can be so deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the V_{CC} capacitor. If this ripple is too large, chances exist to hit the $V_{CC(off)}$ and reset the switcher into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 41 elegantly solves this potential issue by adding an extra capacitor $C_{CC,aux}$ on the auxiliary winding. However, this component is separated from the V_{CC} pin by a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the switcher without affecting the start−up time and standby power.

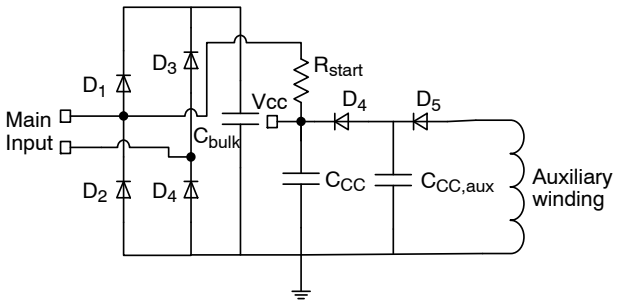


Figure 41. Startup Circuit for NCP112x (half−wave connection), Considering Light Load Condition

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires a change in the traditional type of fixed−frequency operation. NCP112x implement a switching frequency foldback function when the feedback voltage is below $V_{FB(fold)}$. At this point, the oscillator turns into a Voltage−Controlled Oscillator and reduces its switching frequency. The peak current setpoint follows the feedback pin until its level reaches $V_{FB(freeze)}$. Below this value, the peak current freezes to $V_{FB(freeze)}$ / 4. The operating frequency is down to f_{trans} when the feedback voltage reaches $V_{FB(fold,end)}$. Below this point, if the output power continues to decrease, the part enters skip mode for the best noise−free performance in no−load conditions. Figure 6 depicts the adopted scheme for the part.

Over−voltage Protection

The latched−state of the NCP112x is maintained via an internal thyristor (SCR). When the voltage on pin 1 exceeds the latch voltage for four consecutive clock cycles, the SCR is fired and immediately stops the output pulses. The same SCR is fired when an OVP is sensed on the V_{CC} pin. When this happens, all pulses are stopped and V_{CC} is discharged to a fix level of 7 V typically: the circuit is latched and the converter no longer delivers pulses. To maintain the latched−state, a permanent current must be injected in the part. If too low of a current, the part de−latches and the converter resumes operation. This current is characterized to 32 μA as a minimum but we recommend including a design margin and select a value around 60 μA. The test is to latch the part and reduce the input voltage until it de−latches. If you de−latch at V_{in} = 70 V_{rms} for a minimum voltage of 85 V_{rms}, you are fine.

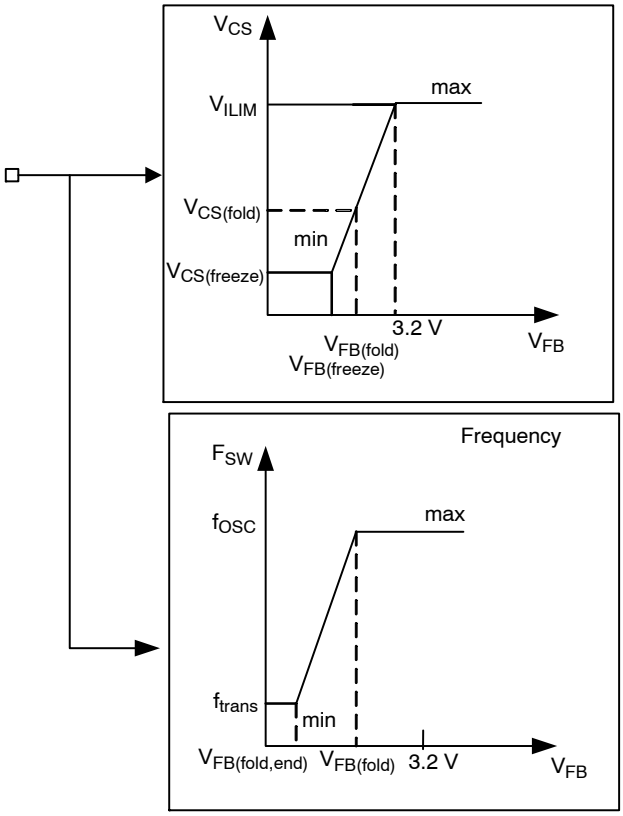


Figure 42. Frequency Foldback Architecture

If it precociously recovers, you will have to increase the start−up current, unfortunately to the detriment of standby power.

The most sensitive configuration is actually that of the half−wave connection proposed in Figure 39. As the current disappears 5 ms for a 10 ms period (50 Hz input source), the latch can potentially open at low line. If you really reduce the start−up current for a low standby power design, you must ensure enough current in the SCR in case of a faulty event. An alternate connection to the above is shown in Figure 43:

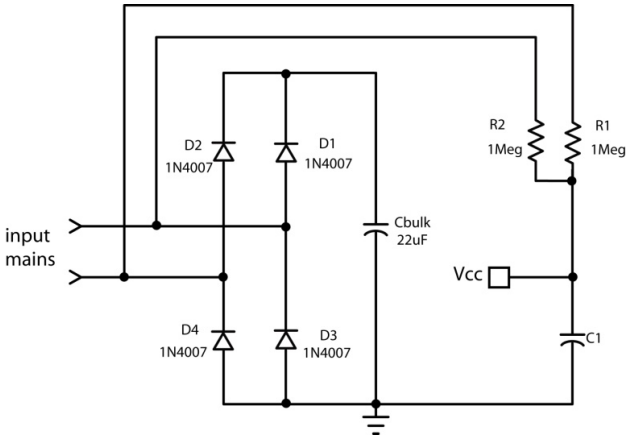


Figure 43. The Full−wave Connection Ensures Latch Current Continuity as Well as a X2−Discharge Path

In this case, the current is no longer made of 5 ms “holes” and the part can be maintained at a low input voltage. Experiments show that these 2−MΩ resistor help to maintain the latch down to less than 50 V rms, giving an excellent design margin. Standby power with this approach was also improved compared to Figure 39 solution. Please note that these resistors also ensure the discharge of the X2−capacitor up to a 0.47 μF type.

The de−latch of the SCR occurs when a) the injected current in the V_{CC} pin falls below the minimum stated in the data−sheet (32 μA at room temp) or when the part senses a brown−out recovery.

Auto−Recovery Short−Circuit Protection

In case of output short−circuit or severe overload situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than t_{OVLD}, the driving pulses are stopped and V_{CC} falls down as the auxiliary pulses are missing. When it hits $V_{CC(off)}$, the switcher consumption is down to a few μA and the V_{CC} slowly builds up again by the startup network R_{start}, C_{CC}. When V_{CC} reaches $V_{CC(on)}$, the switcher purposely ignores the re−start and waits for another V_{CC} cycle: this is the so−called double hiccup. Illustration of such principle appears in Figure 13. Please note that soft−start is activated upon re−start attempt.

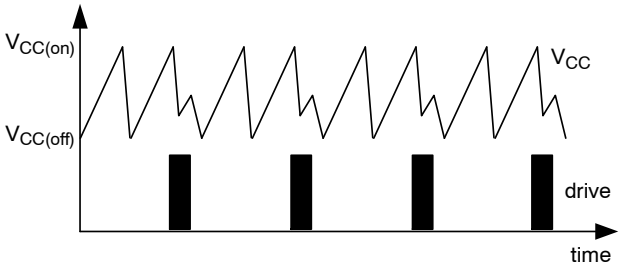


Figure 44. Auto−Recovery Double Hiccup Sequence

Adjustable Ramp Compensation

The NCP112x also include an internal ramp compensation signal. This is the buffered oscillator clock delivered during the on time only. Its amplitude V_{ramp} is around 2.5 V at maximum duty−cycle. Ramp compensation is a well−known method used to eliminate the sub−harmonic oscillations in CCM peak current mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−ratio greater than 50%. To lower the current loop gain, one usually mixes between 50% and 100% of the inductor downslope with the current−sense signal. Figure 45 depicts how internally the ramp is generated. Note that the ramp signal will be disconnected from the CS pin, during the off−time.

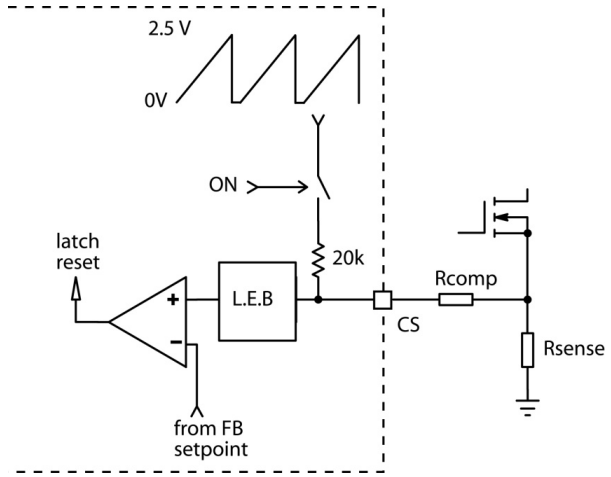


Figure 45. Internal Adjustable Ramp Compensation Architecture

In the NCP112x switchers, the oscillator ramp exhibits a V_{ramp} 2.5 V swing reached at its maximum duty−ratio. If the clock operates at a 65−kHz frequency, then the slope of the ramp is equal to:

$$S_{ramp} = \frac{V_{ramp}}{D_{max} T_{sw}} \quad \text{(eq. 6)}$$

The off−time primary current slope S_p is thus given by Equation 7:

$$S_p = \frac{\left(V_{out} + V_f\right)\frac{N_p}{N_s}}{L_p} \quad \text{(eq. 7)}$$

Given a sense resistor R_{sense} the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p R_{sense} \quad \text{(eq. 8)}$$

The slope of compensation ramp is chosen to be the same as the downslope of the sensing ramp for better transient response. The internal resistor connected to the compensation ramp is 20 kΩ. The series compensation resistor value is therefore:

$$R_{comp} = R_{ramp} \frac{S_{sense}}{S_{ramp}} \quad \text{(eq. 9)}$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin. A100 pF capacitor is recommended to be added to the current sense pin to the switcher ground for improved noise immunity with the current sensing components located very close to the switcher.

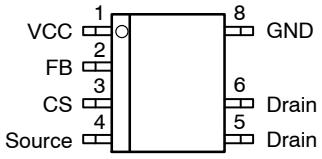
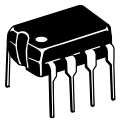


Figure 46. Pin Connections

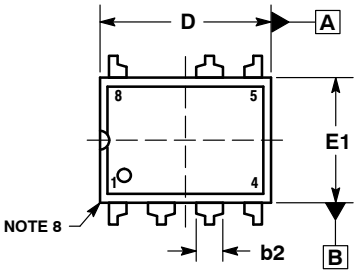
ORDERING INFORMATION

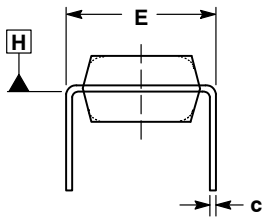
Device	Package	Shipping
NCP1124AP65G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1124BP65G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1124AP100G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1124BP100G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1126AP65G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1126BP65G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1126AP100G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1126BP100G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1129AP65G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1129BP65G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1129AP100G	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1129BP100G	PDIP−7 (Pb−Free)	50 Units / Rail

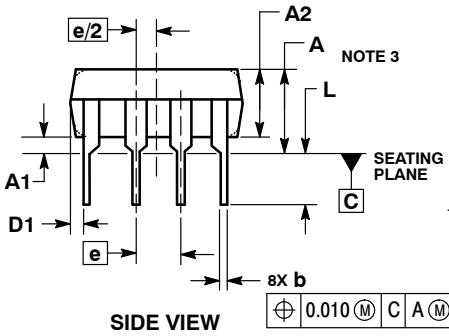


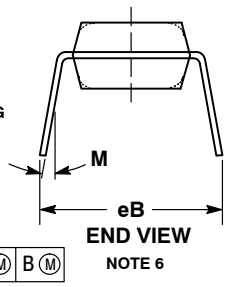
PDIP−7 (PDIP−8 LESS PIN 7)
CASE 626B
ISSUE D

DATE 22 APR 2015







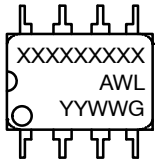


STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. NOT USED
8. V_{CC}

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**PDIP−7 (PDIP−8 LESS PIN 7)**	**PAGE 1 OF 1**

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