

## 3.3 V Automotive Grade LVDS Line Receiver

### NBA3N012C

#### Description

The NBA3N012C is a single LVCMOS Output Differential Line Receiver for Low Power and high data rate Automotive applications. The device is optimized to support data rate higher than 400 Mbps (200 MHz). The NBA3N012C accept directly LVDS signal as an input and translate it to LVCMOS output levels. The device includes an input termination resistor minimizing number of the external components for point to point interface.

The NBA3N012C is offered in 5 lead SOT23 package and it is shipping in 3000 pcs tape & reel.

#### Features

- Compatible with TIA/EIA-644A Standard
- Automotive Grade AECQ-100 Grade 1
- > 400 Mbps (200 MHz) Data Rate
- Operating Range:  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$
- Typical 100 ps Differential Skew
- Maximum Propagation Delay of 3.5 ns
- Low Power Dissipation (Typical 20 mW @ 3.3 V)
- SOT23-5 Lead Package with Pinout optimized for easy PCB Layout
- Integrated Line Termination Resistor of 100  $\Omega$
- Power Down High Impedance on LVDS Pins
- Inputs Accept LVDS/CML/LVPECL Signals
- Temperature Operating Range  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- These are Pb-Free Devices

#### Typical Applications:

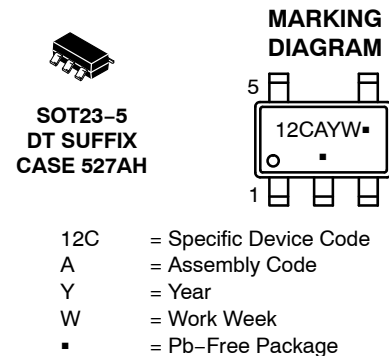
- Automotive: Head Lamp Lighting for Cars
- Telecom: Wireless, Microwave and Optical

Table 1. PIN DESCRIPTION

| Pin Number | Pin Name               | I/O Type | Description             |
|------------|------------------------|----------|-------------------------|
| 1          | $V_{DD}$               |          | Power Supply Pin        |
| 2          | GND                    |          | Ground Pin              |
| 3          | IN                     | Input    | Non-Inverting Input Pin |
| 4          | $\overline{\text{IN}}$ | Input    | Inverting Input Pin     |
| 5          | Q                      | Output   | Output Pin              |

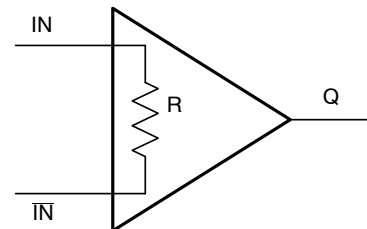
Table 2. TRUTH TABLE

| Inputs                                  | Output |
|-----------------------------------------|--------|
| [IN] – [ $\overline{\text{IN}}$ ]       | Q      |
| $V_{ID} \geq +0.1 \text{ V}$            | H      |
| $V_{ID} \leq -0.1 \text{ V}$            | L      |
| Full Fail Safe OPEN/SHORT or terminated | H or L |

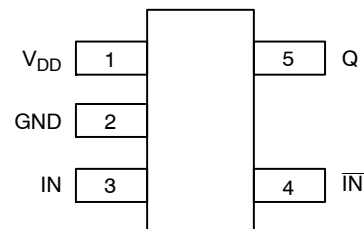


(Note: Microdot may be in either location)

#### LOGIC DIAGRAM



#### PINOUT DIAGRAM



#### ORDERING INFORMATION

| Device         | Package           | Shipping†          |
|----------------|-------------------|--------------------|
| NBA3N012CSNT1G | SOT23-5 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NBA3N012C

**Table 3. ATTRIBUTES** (Note 1)

| Characteristics               |                                                       |          | Value                                 |
|-------------------------------|-------------------------------------------------------|----------|---------------------------------------|
| ESD Protection                | Human Body Model (JEDEC Standard 22, Method A114-E)   | All Pins | $\geq 8$ kV                           |
|                               | Charge Device Model (JEDEC Standard 22, Method C101D) | All Pins | $\geq 1.25$ kV                        |
| Moisture Sensitivity (Note 1) |                                                       |          | Level 1                               |
| Flammability Rating           | Oxygen Index: 28 to 34                                |          | UL 94 Code V-0 A<br>0.125 in 28 to 34 |

1. For additional information, see Application Note AND8003/D

**Table 4. MAXIMUM RATINGS** (Note 2)

| Symbol        | Parameter                                                            | Rating                        | Unit |
|---------------|----------------------------------------------------------------------|-------------------------------|------|
| $V_{DD}$      | Supply voltage                                                       | $-0.30 \leq V_{DD} \leq +4.0$ | V    |
| $V_{IN}$      | Input Voltage (IN, $\overline{IN}$ ) LVDS                            | $-0.30$ to $+3.90$            | V    |
| $V_Q$         | Output Voltage (Pin Q) LVCMOS                                        | $-0.30$ to $(V_{DD} + 0.30)$  | V    |
| $I_{OS}$      | Output Short Circuit Current (Pin Q)                                 | $-100$                        | mA   |
| $T_j$         | Maximum Junction Temperature                                         | 135                           | °C   |
| $T_{stg}$     | Storage Temperature Range                                            | $-65$ to $+150$               | °C   |
| $\theta_{JC}$ | Thermal resistance (Junction-to-Case) – (Note 3)                     | 107                           | °C/W |
| $\theta_{JA}$ | Thermal resistance (Junction-to-Ambient) – (Note 3)                  | 138.5                         | °C/W |
| $T_{sol}$     | Lead Temperature Soldering (4 Seconds) – SOLDERM/D                   | 260                           | °C   |
| PD            | Package Power Dissipation @ 25°C – Derating of 7.22 mW/°C above 25°C | 794                           | mW   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. The maximum ratings applied are individual stress limit values and not valid simultaneously.

3. JEDEC standard multilayer board –2S2P (2 signal 2 power)

**Table 5. DC CHARACTERISTICS**  $V_{DD} = 3.3$  V  $\pm 0.3$  V, GND = 0 V,  $T_A$   $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  (Note 4)

| Symbol   | Parameter                    | Test Conditions                                                              | Min    | Typ    | Max    | Unit |
|----------|------------------------------|------------------------------------------------------------------------------|--------|--------|--------|------|
| $I_{DD}$ | No Load Supply Current       | Pin: $V_{DD}$ ; Inputs Open                                                  |        | 5.4    | 9      | mA   |
| $V_{OH}$ | Output High Voltage          | Pin: Q; $I_{OH} = -0.4$ mA, Inputs shorted or terminated, $V_{ID} = +200$ mV | 2.4    | 3.1    |        | V    |
| $V_{OL}$ | Output Low Voltage           | Pin: Q; $I_{OL} = 2$ mA, $V_{ID} = -200$ mV                                  |        | 0.3    | 0.5    | V    |
| $I_{OS}$ | Output Short Circuit Current | Pin: Q; $V_Q = 0$ V                                                          | $-15$  | $-50$  | $-100$ | mA   |
| $V_{CL}$ | Input Clamp Voltage          | $I_{CL} = -18$ mA                                                            | $-1.5$ | $-0.7$ |        | V    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. – minus sign indicated only direction. Current into the device is defined as positive.  $I_{OS}$  is specified as magnitude only.

**Table 6. ELECTRICAL CHARACTERISTICS**  $V_{DD} = 3.3$  V  $\pm 0.3$  V, GND = 0 V,  $T_A$   $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , Pin: IN/ $\overline{IN}$  (Note 5)

| Symbol           | Parameter                         | Test Conditions                                    |                                | Min  | Typ | Max  | Unit |
|------------------|-----------------------------------|----------------------------------------------------|--------------------------------|------|-----|------|------|
| V <sub>TH</sub>  | Differential Input High Threshold | V <sub>CM</sub> dependent on V <sub>DD</sub>       |                                |      | +30 | +100 | mV   |
| V <sub>TL</sub>  | Differential Input Low Threshold  |                                                    |                                | −100 | −30 |      | mV   |
| V <sub>CM</sub>  | Offset Voltage                    |                                                    |                                | 0.1  |     | 2.35 | V    |
| I <sub>IN</sub>  | Input Current                     | V <sub>IN</sub> = +2.8 V                           | V <sub>DD</sub> = 0 V or 3.6 V | −10  | ±1  | +10  | μA   |
|                  |                                   | V <sub>IN</sub> = 0 V                              |                                | −10  | ±1  | +10  | μA   |
|                  |                                   | V <sub>IN</sub> = +3.6 V                           | V <sub>DD</sub> = 0 V          | −20  |     | +20  | μA   |
| I <sub>IND</sub> | Differential Input Current        | V <sub>IN</sub> = +0.4 V, V <sub>IN</sub> = +0 V   |                                | 3.0  | 3.9 | 4.4  | mA   |
|                  |                                   | V <sub>IN</sub> = +2.4 V, V <sub>IN</sub> = +2.0 V |                                |      |     |      |      |
| R <sub>T</sub>   | Integrated Termination Resistor   |                                                    |                                |      | 100 |      | Ω    |
| C <sub>IN</sub>  | Input Capacitance                 | IN = IN = GND                                      |                                |      | 3   |      | pF   |

5. – minus sign indicated only direction. Current into the device is defined as positive.

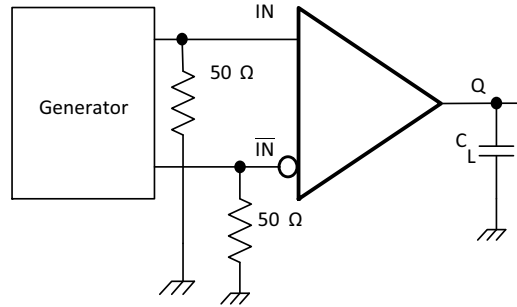
**Table 7. SWITCHING CHARACTERISTICS**

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $GND = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $F = 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r, t_f \leq 3 \text{ ns}$  (0% to 100%) – (Note 6)

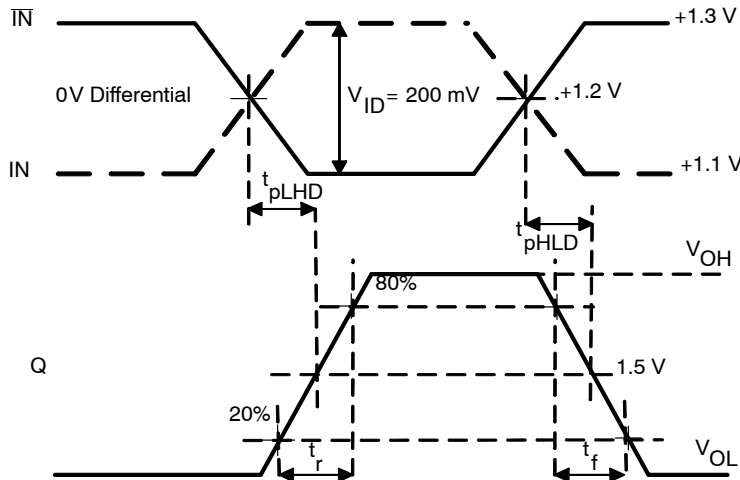
| Symbol         | Parameters                                               | Min | Typ | Max | Unit |
|----------------|----------------------------------------------------------|-----|-----|-----|------|
| $t_{pHLD}$     | High to Low Differential Propagation Delay               | 1.0 | 1.8 | 3.5 | ns   |
| $t_{pLHD}$     | Low to High Differential Propagation Delay               | 1.0 | 1.7 | 3.5 | ns   |
| $t_r$          | Rise Time – Transition Low to High                       |     | 350 | 800 | ps   |
| $t_f$          | Fall Time – Transition High to Low                       |     | 175 | 800 | ps   |
| $t_{SKD(P)}$   | Differential Pulse Skew $ t_{pHLD} - t_{pLHD} $ (Note 7) | 0   | 100 | 400 | ps   |
| $t_{SKD(PP)1}$ | Part to Part Skew – (Note 8)                             | 0   | 0.3 | 1.0 | ns   |
| $t_{SKD(PP)2}$ | Part to Part Skew – (Note 9)                             | 0   | 0.4 | 2.5 | ns   |
| $f_{MAX}$      | Maximum Operating Frequency – (Note 10)                  |     | 250 |     | MHz  |

6. Test Conditions for the above –  $V_{ID} = 200 \text{ mV}$ ,  $C_L = 15 \text{ pF}$  (includes Load & Jig Capacitance), Figures 1 and 2
7.  $|t_{pHLD} - t_{pLHD}|$ , is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
8. Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same  $V_{DD}$  and within  $5^\circ\text{C}$  of each other within the operating temperature range.
9. Part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD2}$  is defined as  $|Max - Min|$  differential propagation delay.
10.  $f_{MAX}$  Input Conditions:  $t_r = t_f < 1 \text{ ns}$  (0% to 100%), Duty Cycle 50%, differential (1.05 V to 1.35 V Peak to Peak).  $f_{MAX}$  Output Conditions:  $V_{OL}$  (Max 0.4 V),  $V_{OH}$  (min 2.4 V), Load = 15 pF (stray + probe), Duty Cycle 60%/40%

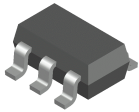
**PARAMETER MEASUREMENT:**



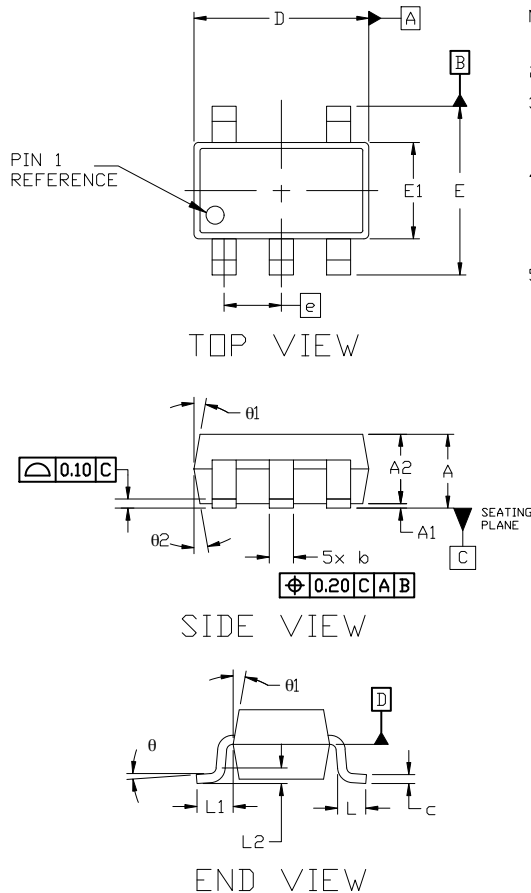
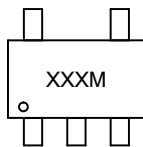
**Figure 1. Receiver Propagation Delay & Transition Time Test Circuit**



**Figure 2. Receiver Propagation Delay & Transition Time Waveforms**


**SOT-23, 5 Lead**  
**CASE 527AH**  
**ISSUE A**

DATE 09 JUN 2021

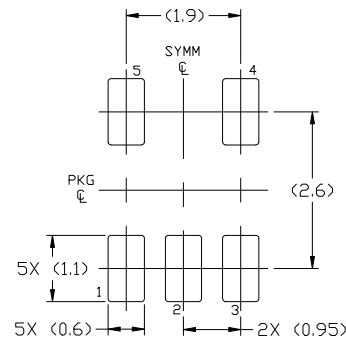

**GENERIC**  
**MARKING DIAGRAM\***

XXX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1989A
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NOM. | MAX. |
| A   | 0.90        | —    | 1.45 |
| A1  | 0.00        | —    | 0.15 |
| A2  | 0.90        | 1.15 | 1.30 |
| b   | 0.30        | —    | 0.50 |
| c   | 0.08        | —    | 0.22 |
| D   | 2.90 BSC    |      |      |
| E   | 2.80 BSC    |      |      |
| E1  | 1.60 BSC    |      |      |
| e   | 0.95 BSC    |      |      |
| L   | 0.30        | 0.45 | 0.60 |
| L1  | 0.60 REF    |      |      |
| L2  | 0.25 REF    |      |      |
| θ   | 0°          | 4°   | 8°   |
| θ1  | 0°          | 10°  | 15°  |
| θ2  | 0°          | 10°  | 15°  |


**RECOMMENDED**  
**MOUNTING FOOTPRINT**

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                       |                                                                                                                                                                                  |
|-------------------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98AON34320E</b>    | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOT-23, 5 LEAD</b> | <b>PAGE 1 OF 1</b>                                                                                                                                                               |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)