

# 3.3 V / 2.5 V / 1.8 V LVCMOS Low Skew Fanout Buffer Family

## NB3V110xC Series

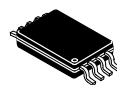
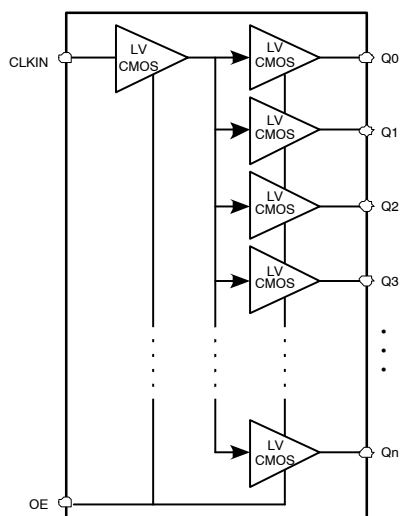
### Description

The NB3V110xC are a modular, high-performance, low-skew, general purpose LVCMOS clock buffer family. The family of devices is designed with a modular approach. Four different fan-out variations, 1:2, 1:3, 1:4, 1:6 and 1:8, are available. All of the devices are pin compatible to each other for easy handling. All family members share the same high performing characteristics like low additive jitter, low skew, and wide operating temperature range. The NB3V110xC supports an asynchronous output enable control (OE) which switches the outputs into a low state when OE is low. The NB3V110xC devices operate in a 3.3 V, 2.5 V and 1.8 V environment and are characterized for operation from  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ .

### Features

- Operating Temperature Range:  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$
- High-Performance 1:2, 1:3, 1:4, 1:6, 1:8 LVCMOS Clock Buffer
- Available in 8-, 14-, 16-Pin TSSOP and WDFN8 Packages
- Very Low Output-to-Output Skew < 50 ps
- Very Low Additive Jitter < 200 fs
- Supply Voltage: 3.3 V, 2.5 V or 1.8 V
- $f_{\text{max}} = 250 \text{ MHz}$  for 3.3 V;  $f_{\text{max}} = 180 \text{ MHz}$  for 2.5 V;  
 $f_{\text{max}} = 133 \text{ MHz}$  for 1.8 V
- These Devices are Pb-Free and are RoHS Compliant

### BLOCK DIAGRAM



TSSOP-8  
DT SUFFIX  
CASE 948S



TSSOP-14  
DT SUFFIX  
CASE 948G

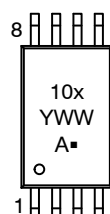


TSSOP-16  
DT SUFFIX  
CASE 948F

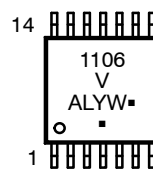


WDFN8, 2x2  
MT SUFFIX  
CASE 511AT

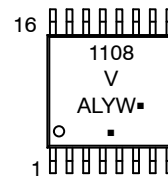
### MARKING DIAGRAMS



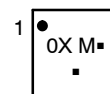
TSSOP-8



TSSOP-14



TSSOP-16



WDFN8

A = Assembly Location  
M = Date Code  
L = Wafer Lot  
Y = Year  
W, WW = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

## NB3V110xC Series

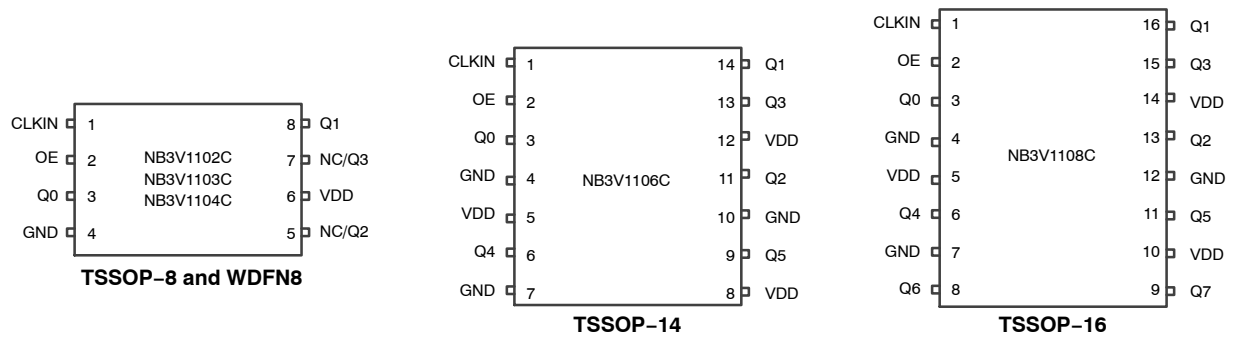


Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION

|           | LVC MOS Clock Input | LVC MOS Clock Output Enable | LVC MOS Clock Output       | Device Supply Voltage | Device Ground |
|-----------|---------------------|-----------------------------|----------------------------|-----------------------|---------------|
| Devices   | CLKIN               | OE                          | Q0, Q1, ... Q7             | V <sub>DD</sub>       | GND           |
| NB3V1102C | 1                   | 2                           | 3, 8                       | 6                     | 4             |
| NB3V1103C | 1                   | 2                           | 3, 8, 5                    | 6                     | 4             |
| NB3V1104C | 1                   | 2                           | 3, 8, 5, 7                 | 6                     | 4             |
| NB3V1106C | 1                   | 2                           | 3, 14, 11, 13, 6, 9        | 5, 8, 12              | 4, 7, 10      |
| NB3V1108C | 1                   | 2                           | 3, 16, 13, 15, 6, 11, 8, 9 | 5, 10, 14             | 4, 7, 12      |

NOTE: Pins not mentioned in the table are NC.

Table 2. OUTPUT LOGIC TABLE

| INPUTS |    | OUTPUTS        |
|--------|----|----------------|
| CLKIN  | OE | Q <sub>n</sub> |
| X      | L  | L              |
| L      | H  | L              |
| H      | H  | H              |

Table 3. ATTRIBUTES

| Characteristic                                                 | Value                                                                                                                | Unit                   |
|----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|------------------------|
| ESD Protection                                                 | Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001-2014<br>Charged Device Model (CDM) per ANSI/ESDA/JEDEC JS-002-2014 | 5000<br>1500<br>V<br>V |
| Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1) | Level 1                                                                                                              | –                      |
| Meets or exceeds JEDEC Spec JESD78D (LU) IC Latchup Test       |                                                                                                                      |                        |

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with a large copper heat spreader (20 mm<sup>2</sup>, 2 oz.)

## NB3V110xC Series

**Table 4. ABSOLUTE MAXIMUM RATINGS** (Note 2)  
**Over operating free-air temperature range (unless otherwise noted)**

| Symbol        | Condition                                 |          | Value                  | Unit |
|---------------|-------------------------------------------|----------|------------------------|------|
| $V_{DD}$      | Supply Voltage Range                      |          | −0.5 to 4.6            | V    |
| $V_{IN}$      | Input Voltage Range (Note 3)              |          | −0.5 to $V_{DD} + 0.5$ | V    |
| $V_O$         | Output Voltage Range (Note 3)             |          | −0.5 to $V_{DD} + 0.5$ | V    |
| $I_{IN}$      | Input Current                             |          | ±20                    | mA   |
| $I_O$         | Continuous Output Current                 |          | ±50                    | mA   |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)  | TSSOP-8  | 151.2*                 | °C/W |
|               |                                           | TSSOP-14 | 104*                   |      |
|               |                                           | TSSOP-16 | 32*                    |      |
|               |                                           |          | 110**                  |      |
|               |                                           | WDFN8    | 190**                  |      |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case top) | TSSOP-8  | 35                     | °C/W |
|               |                                           | TSSOP-14 | 8.6                    |      |
|               |                                           | TSSOP-16 | 10                     |      |
|               |                                           | WDFN8    | 10                     |      |
| $T_J$         | Maximum Junction Temperature              |          | 125                    | °C   |
| $T_{STG}$     | Storage Temperature Range                 |          | −65 to 150             | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with a large copper heat spreader (20 mm<sup>2</sup>, 2 oz.)

3. For additional information, see Application Note AND8003/D.

\*JEDEC51.7 four layer PCB with 100 sqmm, 2 oz with two 80x80x1oz ground planes.

\*\*JEDEC51.3 two layer PCB with 100 sqmm, 2 oz.

## NB3V110xC Series

**Table 5. RECOMMENDED OPERATING CONDITIONS**

Over operating free-air temperature range (unless otherwise noted)

| Symbol                          | Condition                      |                                    | Min                      | Typ | Max                      | Unit |
|---------------------------------|--------------------------------|------------------------------------|--------------------------|-----|--------------------------|------|
| V <sub>DD</sub>                 | Supply voltage range           | 3.3 V supply                       | 3.0                      | 3.3 | 3.6                      | V    |
|                                 |                                | 2.5 V supply                       | 2.3                      | 2.5 | 2.7                      |      |
|                                 |                                | 1.8 V supply                       | 1.71                     | 1.8 | 1.89                     |      |
| V <sub>IL</sub>                 | Low-level input voltage        | V <sub>DD</sub> = 3.0 V to 3.6 V   |                          |     | V <sub>DD</sub> /2 – 600 | mV   |
|                                 |                                | V <sub>DD</sub> = 2.3 V to 2.7 V   |                          |     | V <sub>DD</sub> /2 – 400 |      |
|                                 |                                | V <sub>DD</sub> = 1.71 V to 1.89 V |                          |     | 0.3xV <sub>DD</sub>      | V    |
| V <sub>IH</sub>                 | High-level input voltage       | V <sub>DD</sub> = 3.0 V to 3.6 V   | V <sub>DD</sub> /2 + 600 |     |                          | mV   |
|                                 |                                | V <sub>DD</sub> = 2.3 V to 2.7 V   | V <sub>DD</sub> /2 + 400 |     |                          |      |
|                                 |                                | V <sub>DD</sub> = 1.71 V to 1.89 V | 0.7xV <sub>DD</sub>      |     |                          | V    |
| V <sub>th</sub>                 | Input threshold voltage        | V <sub>DD</sub> = 2.3 V to 3.6 V   | V <sub>DD</sub> /2       |     |                          | V    |
|                                 |                                | V <sub>DD</sub> = 1.71 V to 1.89 V | V <sub>DD</sub> /2       |     |                          | V    |
| t <sub>r</sub> / t <sub>f</sub> | Input slew rate (Note 4)       |                                    | 1                        |     | 4                        | V/ns |
| t <sub>w</sub>                  | Minimum pulse width at CLKIN   | V <sub>DD</sub> = 3.0 V to 3.6 V   | 1.8                      |     |                          | ns   |
|                                 |                                | V <sub>DD</sub> = 2.3 V to 2.7 V   | 2.75                     |     |                          |      |
|                                 |                                | V <sub>DD</sub> = 1.71 V to 1.89 V | 3.75                     |     |                          |      |
| f <sub>CLK</sub>                | LVCMOS clock Input Frequency   | V <sub>DD</sub> = 3.0 V to 3.6 V   | DC                       |     | 250                      | MHz  |
|                                 |                                | V <sub>DD</sub> = 2.3 V to 2.7 V   | DC                       |     | 180                      |      |
|                                 |                                | V <sub>DD</sub> = 1.71 V to 1.89 V | DC                       |     | 133                      |      |
| T <sub>A</sub>                  | Operating free-air temperature |                                    | –40                      |     | 105                      | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Guaranteed by Design.

## NB3V110xC Series

**Table 6. DEVICE CHARACTERISTICS** Over recommended operating free-air temperature range (unless otherwise noted) (Note 5)

| Symbol                                     | Parameter                                         | Condition                                                                                                                            | Min | Typ | Max | Unit |
|--------------------------------------------|---------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| <b>OVERALL PARAMETERS FOR ALL VERSIONS</b> |                                                   |                                                                                                                                      |     |     |     |      |
| I <sub>DD</sub>                            | Static device current                             | OE = V <sub>DD</sub> ; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 3.6 V                               |     |     | 0.2 | mA   |
|                                            |                                                   | OE = V <sub>DD</sub> ; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 2.7 V                               |     |     | 0.2 |      |
|                                            |                                                   | OE = V <sub>DD</sub> ; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 1.89 V                              |     |     | 0.2 |      |
| I <sub>PD</sub>                            | Power down current                                | OE = 0 V; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 3.6 V, 2.7 V or 1.89 V (For 1102C, 1103C, 1104C) |     |     | 60  | μA   |
|                                            |                                                   | OE = 0 V; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 3.6 V, 2.7 V or 1.89 V (For 1106C, 1108C)        |     |     | 75  |      |
| C <sub>PD</sub>                            | Power dissipation capacitance per output (Note 6) | V <sub>DD</sub> = 3.3 V; f = 10 MHz                                                                                                  |     | 9   |     | pF   |
|                                            |                                                   | V <sub>DD</sub> = 2.5 V; f = 10 MHz                                                                                                  |     | 9   |     |      |
|                                            |                                                   | V <sub>DD</sub> = 1.8 V; f = 10 MHz                                                                                                  |     | 9   |     |      |
| I <sub>I</sub>                             | Input leakage current at OE                       | V <sub>I</sub> = 0 V or V <sub>DD</sub> , V <sub>DD</sub> = 3.6 V or 2.7 V                                                           |     |     | ± 8 | μA   |
|                                            | Input leakage current at CLKIN                    |                                                                                                                                      |     |     | ± 8 |      |
|                                            | Input leakage current at OE, CLKIN                | V <sub>I</sub> = 0 V or V <sub>DD</sub> , V <sub>DD</sub> = 1.89 V                                                                   |     |     | ± 8 |      |
| R <sub>OUT</sub>                           | Output impedance                                  | V <sub>DD</sub> = 3.3 V                                                                                                              |     | 40  |     | Ω    |
|                                            |                                                   | V <sub>DD</sub> = 2.5 V                                                                                                              |     | 45  |     |      |
|                                            |                                                   | V <sub>DD</sub> = 1.8 V                                                                                                              |     | 60  |     |      |
| f <sub>OUT</sub>                           | Output frequency                                  | V <sub>DD</sub> = 3.0 V to 3.6 V                                                                                                     | DC  |     | 250 | MHz  |
|                                            |                                                   | V <sub>DD</sub> = 2.3 V to 2.7 V                                                                                                     | DC  |     | 180 |      |
|                                            |                                                   | V <sub>DD</sub> = 1.71 V to 1.89 V                                                                                                   | DC  |     | 133 |      |

### OUTPUT PARAMETERS FOR V<sub>DD</sub> = 3.3 V ± 0.3 V

|                                     |                                                                    |                                                  |      |  |     |    |
|-------------------------------------|--------------------------------------------------------------------|--------------------------------------------------|------|--|-----|----|
| V <sub>OH</sub>                     | High-level output voltage                                          | V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -0.1 mA | 2.9  |  |     | V  |
|                                     |                                                                    | V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -8 mA   | 2.5  |  |     |    |
|                                     |                                                                    | V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -12 mA  | 2.2  |  |     |    |
| V <sub>OL</sub>                     | Low-level output voltage                                           | V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 0.1 mA  |      |  | 0.1 | V  |
|                                     |                                                                    | V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 8 mA    |      |  | 0.5 |    |
|                                     |                                                                    | V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 12 mA   |      |  | 0.8 |    |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay (Note 7)                                         | CLKIN to Qn                                      | 0.8  |  | 2.0 | ns |
| t <sub>sk(o)</sub>                  | Output skew (Note 7)                                               | Equal load of each output 85°C                   |      |  | 50  | ps |
|                                     |                                                                    | Equal load of each output 105°C                  |      |  | 60  |    |
| t <sub>r</sub> /t <sub>f</sub>      | Rise and fall time                                                 | 20%–80% (V <sub>OH</sub> - V <sub>OL</sub> )     | 0.12 |  | 0.8 | ns |
| t <sub>DIS</sub>                    | Output disable time (Note 7)                                       | OE to Qn                                         |      |  | 6   | ns |
| t <sub>EN</sub>                     | Output enable time (Note 7)                                        | OE to Qn                                         |      |  | 6   | ns |
| t <sub>sk(p)</sub>                  | Pulse skew; t <sub>PLH</sub> (Qn) - t <sub>PHL</sub> (Qn) (Note 8) | To be measured with input duty cycle of 50%      |      |  | 180 | ps |
| t <sub>sk(pp)</sub>                 | Part-to-part skew                                                  | Under equal operating conditions for two parts   |      |  | 0.5 | ns |
| T <sub>jitt(φ)</sub>                | Additive jitter rms                                                | 12 kHz...20 MHz f <sub>OUT</sub> = 100 MHz       |      |  | 100 | fs |
|                                     |                                                                    | 12 kHz...20 MHz f <sub>OUT</sub> = 156.25 MHz    |      |  |     |    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All typical values are at respective nominal V<sub>DD</sub>. For switching characteristics, outputs are terminated to 50 Ω to V<sub>DD</sub>/2 (see Figure 2).

6. This is the formula for the power dissipation calculation.

$$P_{tot} = P_{stat} + P_{dyn} + P_{Cload} [W] \quad P_{stat} = V_{DD} \times I_{DD} [W]$$

$$P_{dyn} = C_{PD} \times V_{DD}^2 \times f \times n [W]$$

$$P_{Cload} = C_{load} \times V_{DD}^2 \times f \times n [W]$$

n = Number of switching output pins

7. With rail to rail input clock.

8. t<sub>sk(p)</sub> depends on output rise- and fall-time (t<sub>r</sub>/t<sub>f</sub>). The output duty-cycle can be calculated: odc = (t<sub>w(OUT)</sub> ± t<sub>sk(p)</sub>)/t<sub>period</sub>; t<sub>w(OUT)</sub> is pulse-width of ideal output waveform and t<sub>period</sub> is 1/f<sub>OUT</sub>.

## NB3V110xC Series

**Table 7. DEVICE CHARACTERISTICS (continued)**

Over recommended operating free-air temperature range (unless otherwise noted) (Note 5)

| Symbol                                                                             | Parameter                                         | Condition                                             | Min  | Typ | Max | Unit |
|------------------------------------------------------------------------------------|---------------------------------------------------|-------------------------------------------------------|------|-----|-----|------|
| <b>OUTPUT PARAMETERS FOR <math>V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}</math></b> |                                                   |                                                       |      |     |     |      |
| $V_{OH}$                                                                           | High-level output voltage                         | $V_{DD} = 2.3 \text{ V}$ , $I_{OH} = -0.1 \text{ mA}$ | 2.2  |     |     | V    |
|                                                                                    |                                                   | $V_{DD} = 2.3 \text{ V}$ , $I_{OH} = -8 \text{ mA}$   | 1.7  |     |     |      |
| $V_{OL}$                                                                           | Low-level output voltage                          | $V_{DD} = 2.3 \text{ V}$ , $I_{OL} = 0.1 \text{ mA}$  |      |     | 0.1 | V    |
|                                                                                    |                                                   | $V_{DD} = 2.3 \text{ V}$ , $I_{OL} = 8 \text{ mA}$    |      |     | 0.5 |      |
| $t_{PLH}$ , $t_{PHL}$                                                              | Propagation delay (Note 10)                       | CLKIN to Qn                                           |      | 1.8 |     | ns   |
| $t_{sk(o)}$                                                                        | Output skew (Note 10)                             | Equal load of each output 85°C                        |      |     | 50  | ps   |
|                                                                                    |                                                   | Equal load of each output 105°C                       |      |     | 60  |      |
| $t_r/t_f$                                                                          | Rise and fall time                                | 20%–80% ( $V_{OH} - V_{OL}$ )                         | 0.12 |     | 1.2 | ns   |
| $t_{DIS}$                                                                          | Output disable time (Note 10)                     | OE to Qn                                              |      |     | 10  | ns   |
| $t_{EN}$                                                                           | Output enable time (Note 10)                      | OE to Qn                                              |      |     | 10  | ns   |
| $t_{sk(p)}$                                                                        | Pulse skew ; $t_{PLH(Qn)} - t_{PHL(Qn)}$ (Note 9) | To be measured with input duty cycle of 50%           |      |     | 220 | ps   |
| $t_{sk(pp)}$                                                                       | Part-to-part skew                                 | Under equal operating conditions for two parts        |      |     | 1.2 | ns   |
| $t_{jit(\phi)}$                                                                    | Additive jitter rms                               | 12 kHz...20 MHz $f_{OUT} = 100 \text{ MHz}$           |      |     | 150 | fs   |
|                                                                                    |                                                   | 12 kHz...20 MHz $f_{OUT} = 156.25 \text{ MHz}$        |      |     | 100 |      |

**OUTPUT PARAMETERS FOR  $V_{DD} = 1.8 \text{ V} \pm 5\%$**

|                       |                                                   |                                                        |                      |  |                      |    |
|-----------------------|---------------------------------------------------|--------------------------------------------------------|----------------------|--|----------------------|----|
| $V_{OH}$              | High-level output voltage                         | $V_{DD} = 1.71 \text{ V}$ , $I_{OH} = -0.1 \text{ mA}$ | 1.6                  |  |                      | V  |
|                       |                                                   | $V_{DD} = 1.71 \text{ V}$ , $I_{OH} = -4 \text{ mA}$   | $0.75 \times V_{DD}$ |  |                      |    |
| $V_{OL}$              | Low-level output voltage                          | $V_{DD} = 1.71 \text{ V}$ , $I_{OL} = 0.1 \text{ mA}$  |                      |  | 0.1                  | V  |
|                       |                                                   | $V_{DD} = 1.71 \text{ V}$ , $I_{OL} = 4 \text{ mA}$    |                      |  | $0.25 \times V_{DD}$ |    |
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay (Note 10)                       | CLKIN to Qn                                            | 1.8                  |  | 3.5                  | ns |
| $t_{sk(o)}$           | Output skew (Note 10)                             | Equal load of each output                              |                      |  | 75                   | ps |
| $t_r/t_f$             | Rise and fall time                                | 20%–80% ( $V_{OH} - V_{OL}$ )                          | 0.17                 |  | 1.2                  | ns |
| $t_{DIS}$             | Output disable time (Note 10)                     | OE to Qn                                               |                      |  | 10                   | ns |
| $t_{EN}$              | Output enable time (Note 10)                      | OE to Qn                                               |                      |  | 10                   | ns |
| $t_{sk(p)}$           | Pulse skew ; $t_{PLH(Qn)} - t_{PHL(Qn)}$ (Note 9) | To be measured with input duty cycle of 50%            |                      |  | 450                  | ps |
| $t_{sk(pp)}$          | Part-to-part skew                                 | Under equal operating conditions for two parts         |                      |  | 1.2                  | ns |
| $t_{jit(\phi)}$       | Additive jitter rms                               | 12 kHz...20 MHz, $f_{OUT} = 100 \text{ MHz}$           |                      |  | 200                  | fs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9.  $t_{sk(p)}$  depends on output rise- and fall-time ( $t_r/t_f$ ). The output duty-cycle can be calculated:  $odc = (t_{w(OUT)} \pm t_{sk(p)})/t_{period}$ ;  $t_{w(OUT)}$  is pulse-width of ideal output waveform and  $t_{period}$  is  $1/f_{OUT}$ .

10. With rail to rail input clock.

# NB3V110xC Series

## PARAMETERS MEASUREMENT INFORMATION

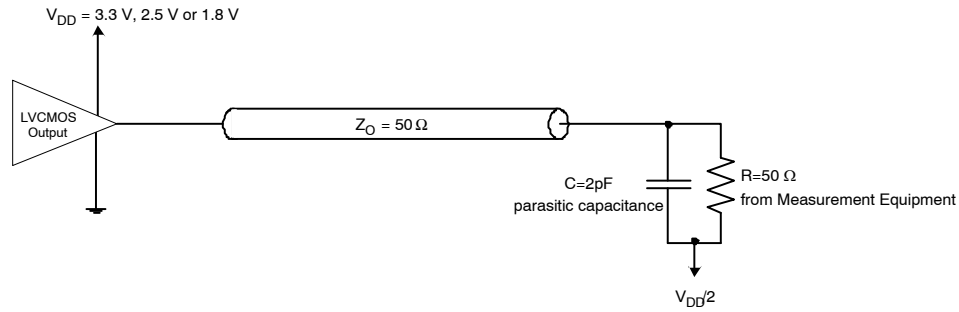


Figure 2. Test Load Circuit

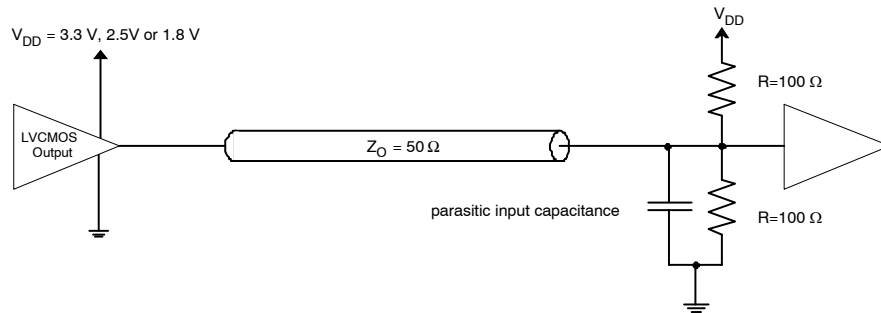


Figure 3. Application Load with  $50\ \Omega$  Line Termination

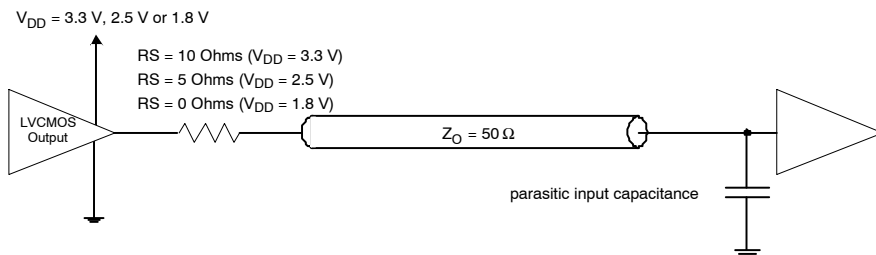


Figure 4. Application Load with Series Line Termination

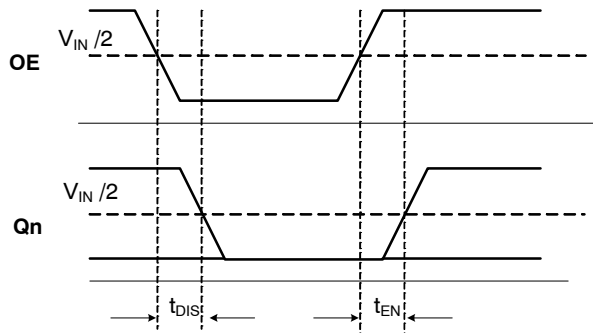


Figure 5.  $t_{DIS}$  and  $t_{EN}$  for Disable Low

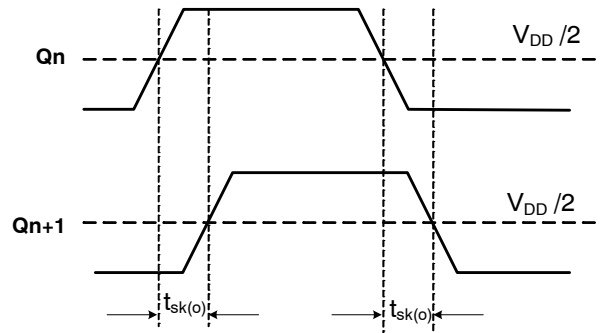
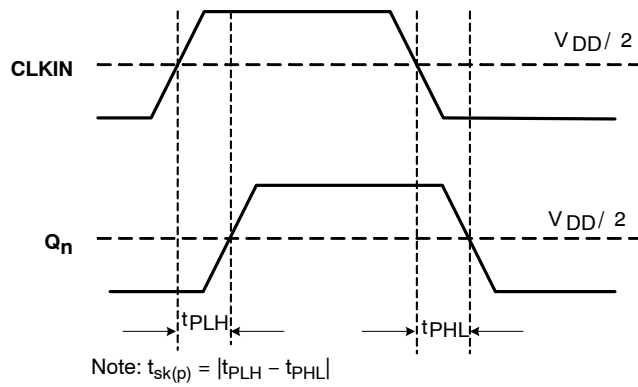
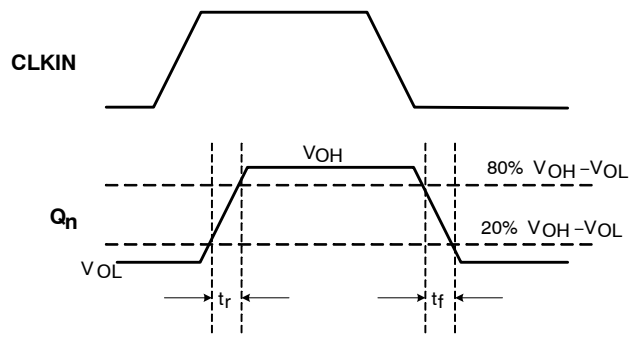


Figure 6. Output Skew  $t_{sk(o)}$

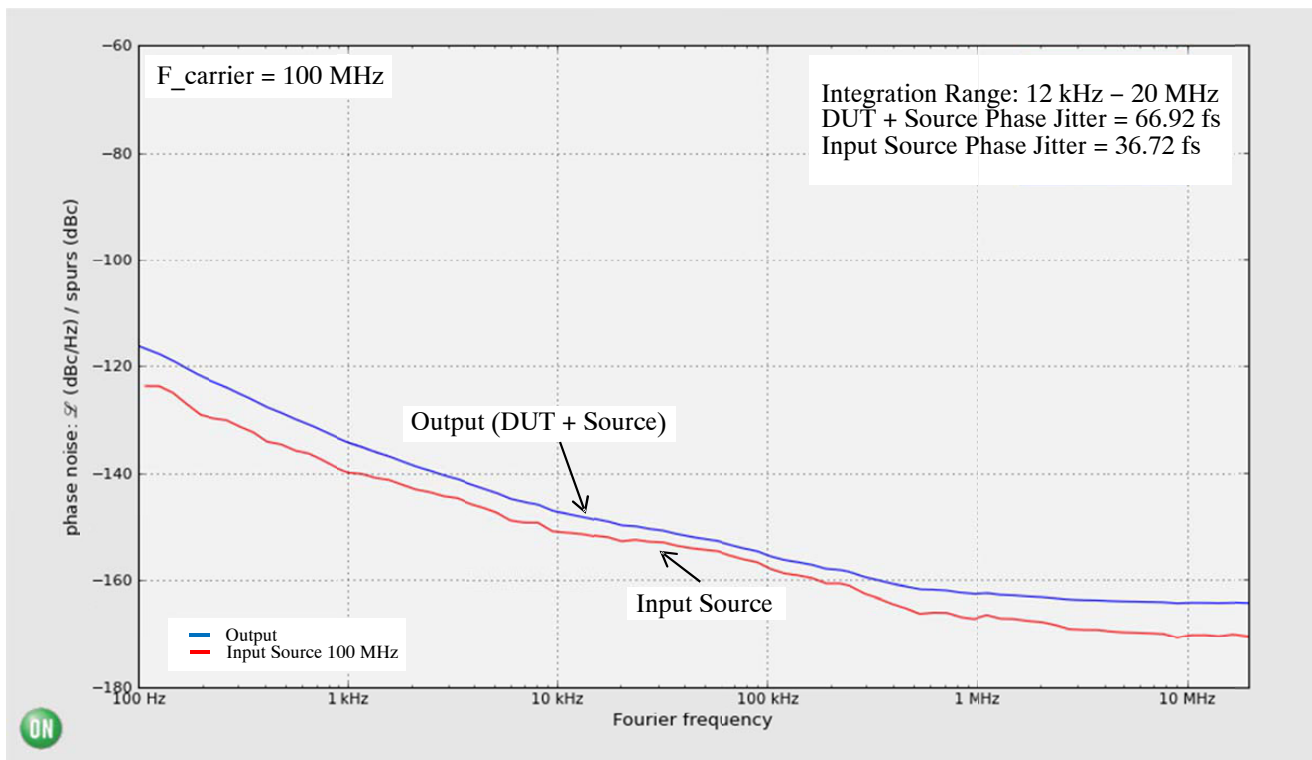
## NB3V110xC Series



**Figure 7. Pulse Skew  $t_{sk(p)}$  and Propagation Delay  $t_{PLH}/t_{PHL}$**



**Figure 8. Rise/Fall Times  $t_r/t_f$**



**Figure 9. Typical NB3V110xC Phase Noise Plot at  $f_{Carrier} = 100$  MHz,  $V_{DD} = 3.3$  V,  $25^\circ\text{C}$**

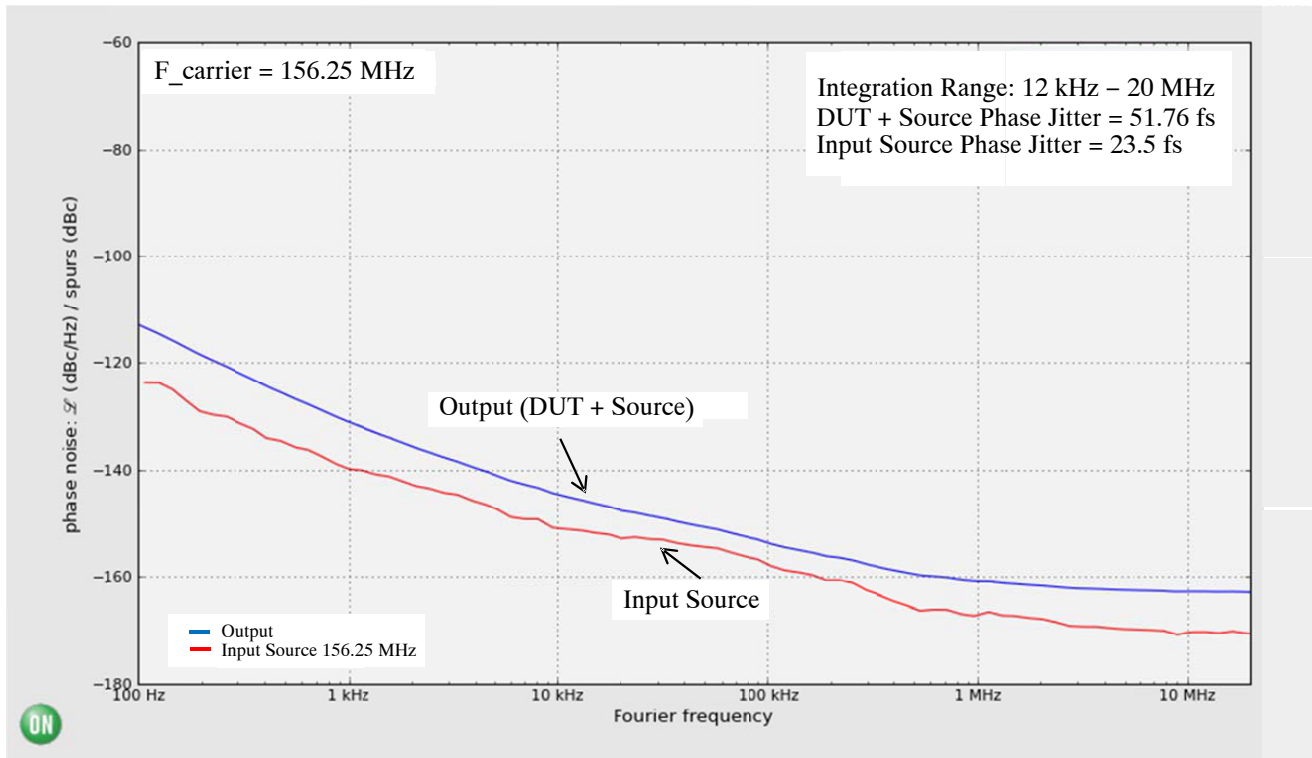
The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 55.94 fs. The additive RMS phase jitter performance of the fan out buffer is highly dependent on the phase noise of the input source.

To obtain the most precise additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is greater than the noise floor of the device under test, the source noise will dominate the additive phase jitter calculation and lead to an incorrect negative result for the additive phase noise within the integration range. The Figure above is a good example of the NB3V110xC source generator phase noise having a significantly lower floor than the DUT and results in an additive phase jitter of 55.94 fs.

$$\text{Additive RMS phase jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$55.94 \text{ fs} = \sqrt{66.92 \text{ fs}^2 - 36.72 \text{ fs}^2}$$

## NB3V110xC Series



**Figure 10. Typical NB3V110xC Phase Noise Plot at  $f_{\text{carrier}} = 156.25 \text{ MHz}$ ,  $V_{\text{CC}} = 3.3 \text{ V V}$ ,  $25^\circ\text{C}$**

The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 46.11 fs.

$$\begin{aligned} \text{Additive RMS phase jitter} &= \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2} \\ 46.11 \text{ fs} &= \sqrt{51.76 \text{ fs}^2 - 23.5 \text{ fs}^2} \end{aligned}$$

Figures 9 and 10 were created with measured data from Agilent-E5052A/B Signal Source Analyzer using **onsemi** Phase Noise Explorer web tool. This free application enables an interactive environment for advanced phase

noise and jitter analysis of timing devices and clock tree designs. To see the performance of NB3V110xC beyond conditions outlined in this datasheet, please visit the **onsemi** Green Point Design Tools homepage.

**Table 8. ORDERING INFORMATION**

| Device         | Marking   | Package               | Shipping <sup>†</sup> |
|----------------|-----------|-----------------------|-----------------------|
| NB3V1102CDTR2G | 102       | TSSOP-8<br>(Pb-Free)  | 2500 / Tape & Reel    |
| NB3V1103CDTR2G | 103       |                       |                       |
| NB3V1104CDTR2G | 104       |                       |                       |
| NB3V1102CMTTBG | 02        | WDFN8<br>(Pb-Free)    | 3000 / Tape & Reel    |
| NB3V1104CMTTBG | 04        |                       |                       |
| NB3V1106CDTR2G | 1106<br>V | TSSOP-14<br>(Pb-Free) | 2500 / Tape & Reel    |
| NB3V1108CDTR2G | 1108<br>V | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

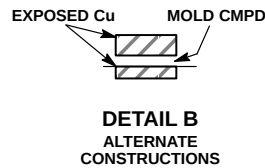
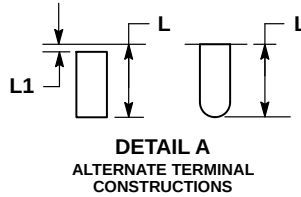
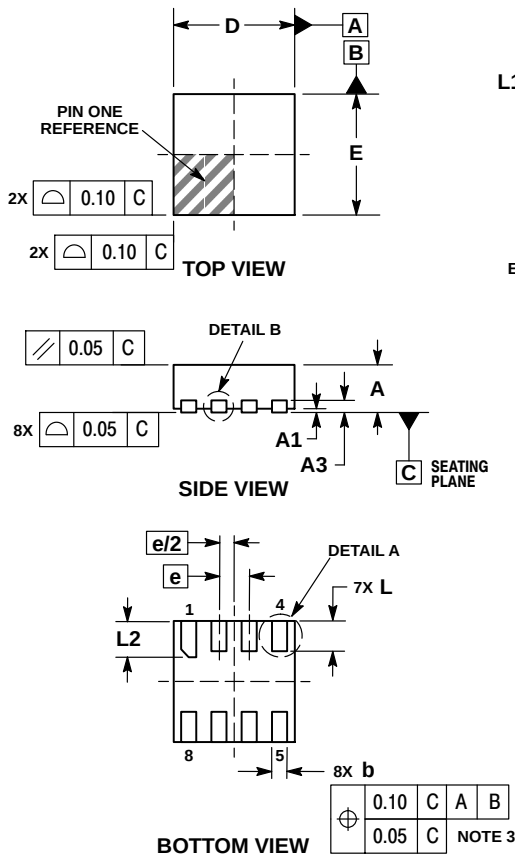
NOTE: Please contact your **onsemi** sales representative for availability of parts in tube.



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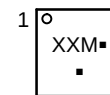
**WDFN8 2x2, 0.5P**  
**CASE 511AT**  
**ISSUE O**

DATE 26 FEB 2010


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

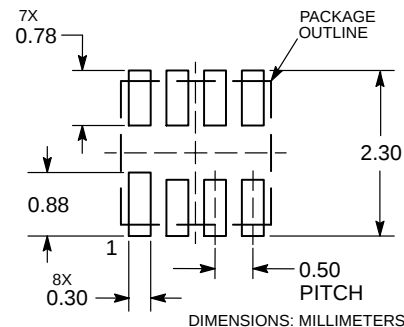
| MILLIMETERS |          |      |
|-------------|----------|------|
| DIM         | MIN      | MAX  |
| A           | 0.70     | 0.80 |
| A1          | 0.00     | 0.05 |
| A3          | 0.20 REF |      |
| b           | 0.20     | 0.30 |
| D           | 2.00 BSC |      |
| E           | 2.00 BSC |      |
| e           | 0.50 BSC |      |
| L           | 0.40     | 0.60 |
| L1          | ---      | 0.15 |
| L2          | 0.50     | 0.70 |

**GENERIC MARKING DIAGRAM\***


XX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Device

(Note: Microdot may be in either location)

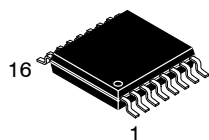
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**RECOMMENDED SOLDERING FOOTPRINT\***


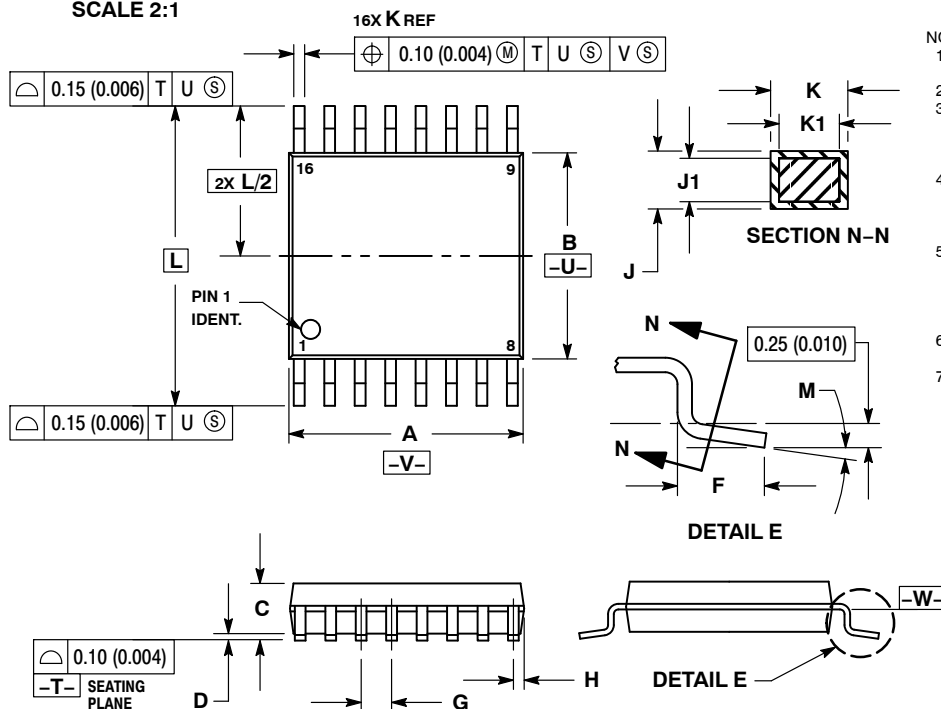
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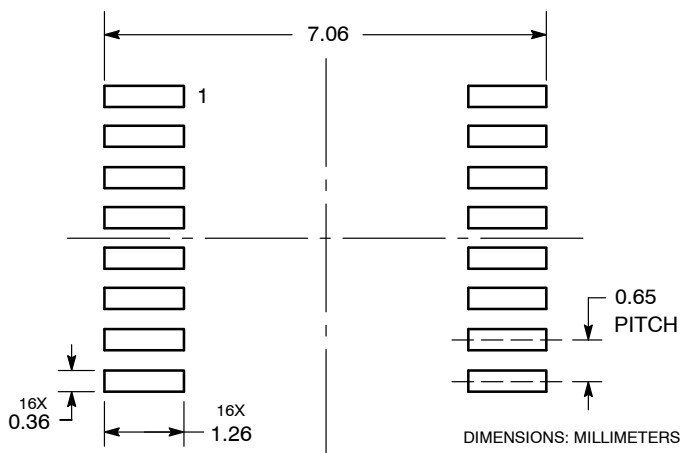

**TSSOP-16 WB**  
**CASE 948F**  
**ISSUE B**

DATE 19 OCT 2006

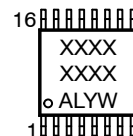

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

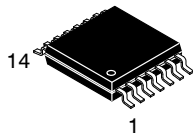
**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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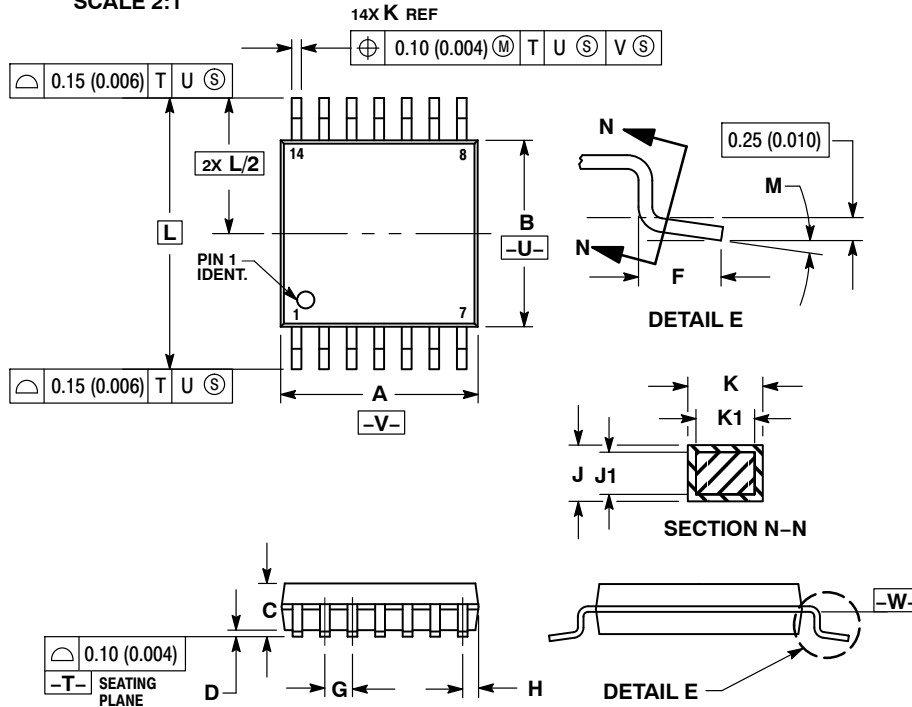
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TSSOP-14 WB  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

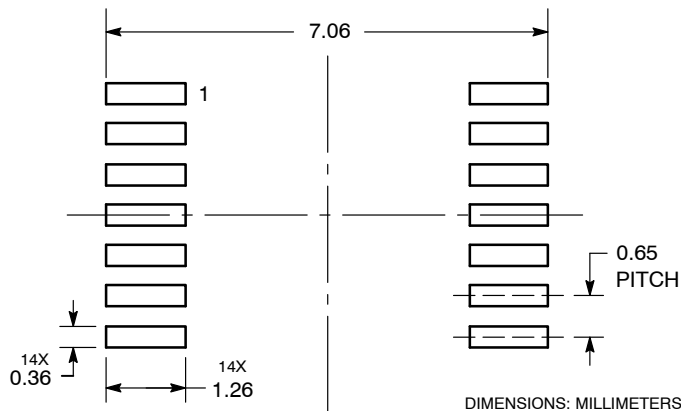


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

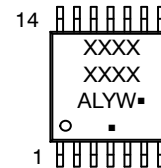
| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

RECOMMENDED  
SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

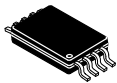
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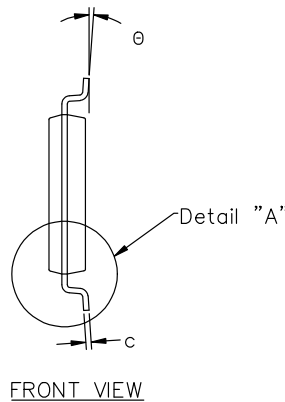
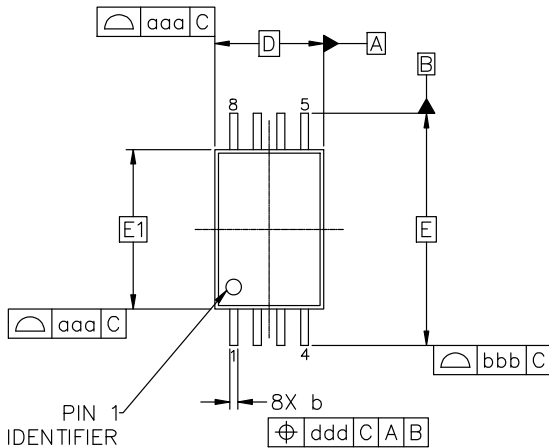
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TSSOP-8 3.00x4.00x0.90, 0.65P  
CASE 948S  
ISSUE D

DATE 24 OCT 2025

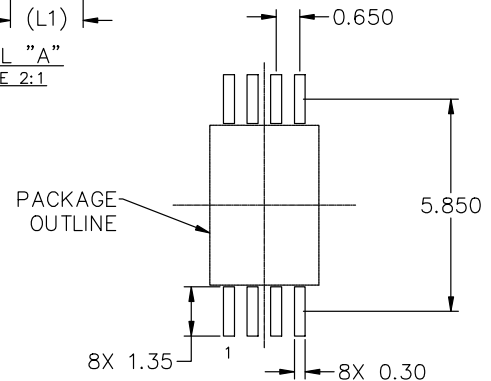
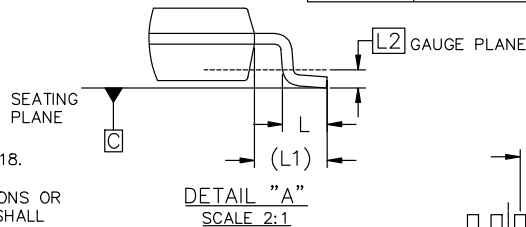
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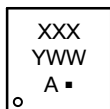
| MILLIMETERS               |          |      |      |
|---------------------------|----------|------|------|
| DIM                       | MIN      | NOM  | MAX  |
| A                         | 0.90     | 1.00 | 1.10 |
| A1                        | 0.05     | 0.10 | 0.15 |
| A2                        | 0.80     | 0.90 | 1.00 |
| b                         | 0.19     | 0.25 | 0.30 |
| c                         | 0.09     | 0.15 | 0.20 |
| D                         | 3.00 BSC |      |      |
| E                         | 6.40 BSC |      |      |
| E1                        | 4.40 BSC |      |      |
| L                         | 0.50     | 0.60 | 0.70 |
| L1                        | 1.00 REF |      |      |
| L2                        | 0.25 BSC |      |      |
| θ                         | 0°       | 4°   | 8°   |
| TOLERANCE FORM & POSITION |          |      |      |
| aaa                       | 0.10     |      |      |
| bbb                       | 0.20     |      |      |
| ccc                       | 0.10     |      |      |
| ddd                       | 0.10     |      |      |
| eee                       | 0.05     |      |      |

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07mm.



GENERIC  
MARKING DIAGRAM\*



XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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