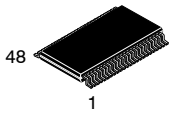
Low-Voltage CMOS 16-Bit Transparent Latch

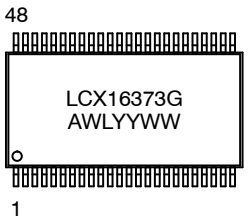
With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16373



TSSOP-48
DT SUFFIX
CASE 1201

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

The MC74LCX16373 is a high performance, non-inverting 16-bit transparent latch operating from a 1.65 V to 5.5 V supply. The device is byte controlled. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX16373 inputs to be safely driven from 5.0 V devices.

The MC74LCX16373 contains 16 D-type latches with 3-state 5.0 V-tolerant outputs. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state outputs are controlled by the Output Enable ($\overline{OEn}$) inputs. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

Features

- Designed for 1.65 to 5.5 V V_{CC} Operation
- 5.4 ns Maximum t_{pd}
- 5.0 V Tolerant – Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability at V_{CC} = 3 V
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
  - Human Body Model >2000 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

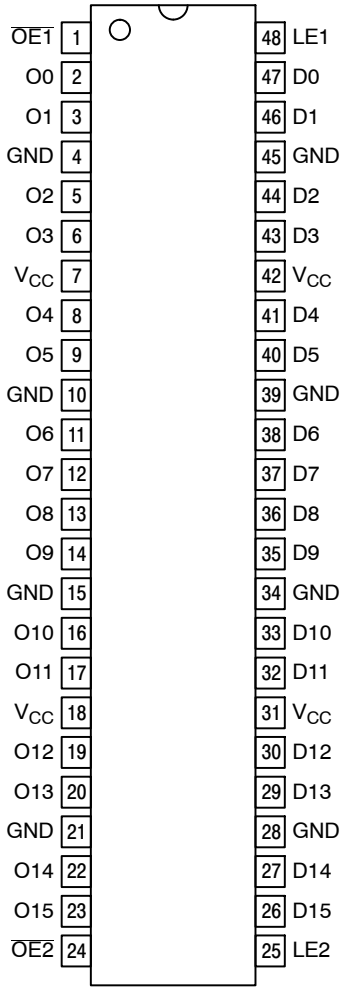


Figure 1. Pinout: 48-Lead
(Top View)

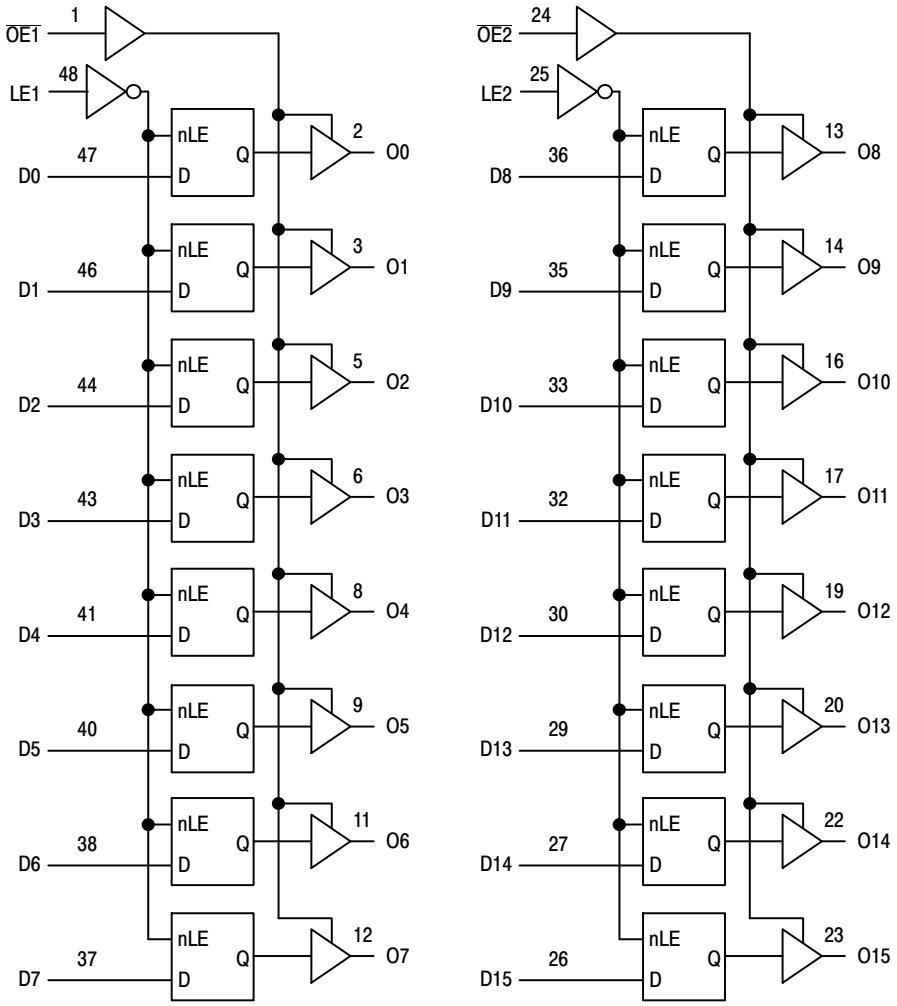


Figure 2. Logic Diagram

Table 1. PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
LEn	Latch Enable Inputs
D0–D15	Inputs
O0–O15	Outputs

TRUTH TABLE

Inputs			Outputs	Inputs			Outputs
LE1	**$\overline{OE1}$**	**D0:7**	**O0:7**	**LE2**	**$\overline{OE2}$**	**D8:15**	**O8:15**
X	H	X	Z	X	H	X	Z
H	L	L	L	H	L	L	L
H	L	H	H	H	L	H	H
L	L	X	O0	L	L	X	O0

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions Are Acceptable; for I_{CC} reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +6.5	V
V_{IN}	DC Input Voltage (Note 1)		–0.5 to +6.5	V
V_{OUT}	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V_{CC} = 0 V)	–0.5 to V_{CC} + 0.5 –0.5 to +6.5 –0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	–50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	–50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Supply Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		71	°C/W
P_D	Power Dissipation in Still Air		1765	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	>2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	2.5, 3.3 2.5, 3.3	5.5 5.5	V
V_{IN}	Digital Input Voltage		0		5.5	V
V_{OUT}	Output Voltage	Active Mode (High or Low State) Tri-State Mode Power Down Mode (V_{CC} = 0 V)	0 0 0		V_{CC} 5.5 5.5	V
T_A	Operating Free-Air Temperature		–55		+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V V_{CC} = 4.5 V to 5.5 V	0 0 0 0		20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40 °C to +85 °C		T_A = −55 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 x V_{CC}		0.65 x V_{CC}		V
			2.3 to 2.7	1.7		1.7		
			2.7 to 3.6	2.0		2.0		
			4.5 to 5.5	0.7 x V_{CC}		0.7 x V_{CC}		
V_{IL}	Low-Level Input Voltage		1.65 to 1.95		0.35 x V_{CC}		0.35 x V_{CC}	V
			2.3 to 2.7		0.7		0.7	
			2.7 to 3.6		0.8		0.8	
			4.5 to 5.5		0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	High-Level Output Voltage	V_I = V_{IH} or V_{IL} I_{OH} = −100 μA I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V_{CC} − 0.1 1.2 1.8 2.2 2.4 2.2 3.8		V_{CC} − 0.1 1.2 1.8 2.2 2.4 2.2 3.8		V
V_{OL}	Low-Level Output Voltage	V_I = V_{IH} or V_{IL} I_{OH} = −100 μA I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.1 0.45 0.6 0.4 0.4 0.55 0.6		0.1 0.45 0.6 0.4 0.4 0.55 0.6	V
I_I	Input Leakage Current	V_I = 0 to 5.5 V	3.6		±5.0		±5.0	μA
I_{OZ}	3-State Output Leakage Current	V_I = V_{IH} or V_{IL}, V_O = 0 V to 5.5 V	3.6		±5.0		±5.0	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0		10		10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	3.6		10		10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6 V	2.3 to 3.6		500		500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = −40 °C to +85 °C		T_A = −55 °C to +125 °C		Unit
				Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, D_n to O_n	See Figures 3 and 4, Waveform 1	1.65 to 1.95		11.4		11.4	ns
			2.3 to 2.7		6.5		6.5	
			2.7		5.9		5.9	
			3.0 to 3.6		5.4		5.4	
			4.5 to 5.5		5.4		5.4	
t_{PLH}, t_{PHL}	Propagation Delay, LE to O_n	See Figures 3 and 4, Waveform 3	1.65 to 1.95		12.4		12.4	ns
			2.3 to 2.7		6.6		6.6	
			2.7		6.4		6.4	
			3.0 to 3.6		5.5		5.5	
			4.5 to 5.5		5.5		5.5	
t_{PZH}, t_{PZL}	Output Enable Time, $\overline{OE}$ to O	See Figures 3 and 4, Waveform 2	1.65 to 1.95		12.4		12.4	ns
			2.3 to 2.7		7.9		7.9	
			2.7		6.5		6.5	
			3.0 to 3.6		6.1		6.1	
			4.5 to 5.5		6.1		6.1	
t_{PHZ}, t_{PLZ}	Output Disable Time, $\overline{OE}$ to O	See Figures 3 and 4, Waveform 2	1.65 to 1.95		9.1		9.1	ns
			2.3 to 2.7		7.2		7.2	
			2.7		6.3		6.3	
			3.0 to 3.6		6.0		6.0	
			4.5 to 5.5		6.0		6.0	
t_s	Setup Time, High or Low D_n to LE	See Figures 3 and 4, Waveform 3	1.65 to 1.95	3.0		3.0		ns
			2.3 to 2.7	3.0		3.0		
			2.7	2.5		2.5		
			3.0 to 3.6	2.5		2.5		
			4.5 to 5.5	2.5		2.5		
t_h	Hold Time, High or Low D_n to LE	See Figures 3 and 4, Waveform 3	1.65 to 1.95	2.5		2.5		ns
			2.3 to 2.7	2.0		2.0		
			2.7	1.5		1.5		
			3.0 to 3.6	1.5		1.5		
			4.5 to 5.5	1.5		1.5		
t_w	LE Pulse Width, High	See Figures 3 and 4, Waveform 3	1.65 to 1.95	5.0		5.0		ns
			2.3 to 2.7	3.5		3.5		
			2.7	3.0		3.0		
			3.0 to 3.6	3.0		3.0		
			4.5 to 5.5	3.0		3.0		
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 5)		1.65 to 1.95		1.0		1.0	ns
			2.3 to 2.7		1.0		1.0	
			2.7		1.0		1.0	
			3.0 to 3.6		1.0		1.0	
			4.5 to 5.5		1.0		1.0	

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (tOSHL) or LOW-to-HIGH (tOSLH); parameter guaranteed by design.

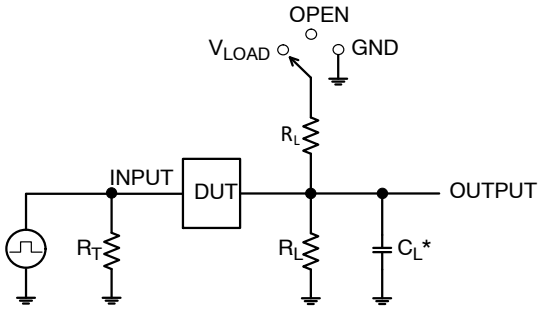
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25 °C			Units
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 6)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		0.8 0.6		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 6)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		−0.8 −0.6		V

6. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

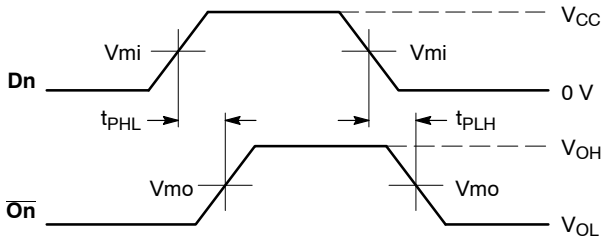
Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	20	pF



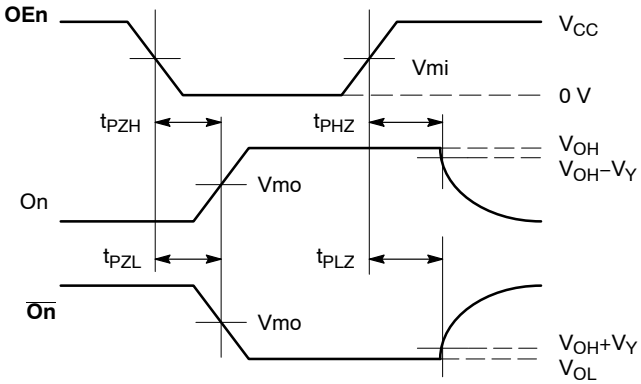
Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

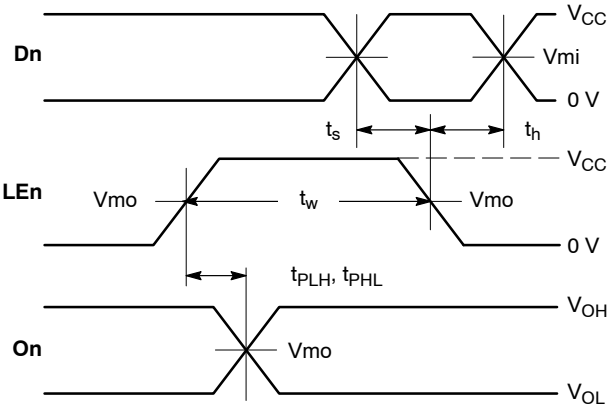
Figure 3. Test Circuit



WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns except when noted

Figure 4. AC Waveforms

V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_{mi}, V	V_{mo}, V	V_Y, V
1.65 to 1.95	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.3 to 2.7	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.7	500	50	6 V	1.5	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	1.5	0.3
4.5 to 4.5	500	50	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.3

ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX16373DTG	TSSOP-48 (Pb-Free)	39 Units / Rail
MC74LCX16373DTR2G	TSSOP-48 (Pb-Free)	2500 / Tape & Reel
MC74LCX16373DTR2G-Q*	TSSOP-48 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*–Q Suffx for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

REVISION HISTORY

Revision	Description of Changes	Date
13	Five value edits on page 1, remove one bullet and edit another, update and move order info table, replace all tables on pages 3 and 4, add a new figure 3 and waveform table	10/27/2025
14	Edits to the EC table on page 5	3/2/2026

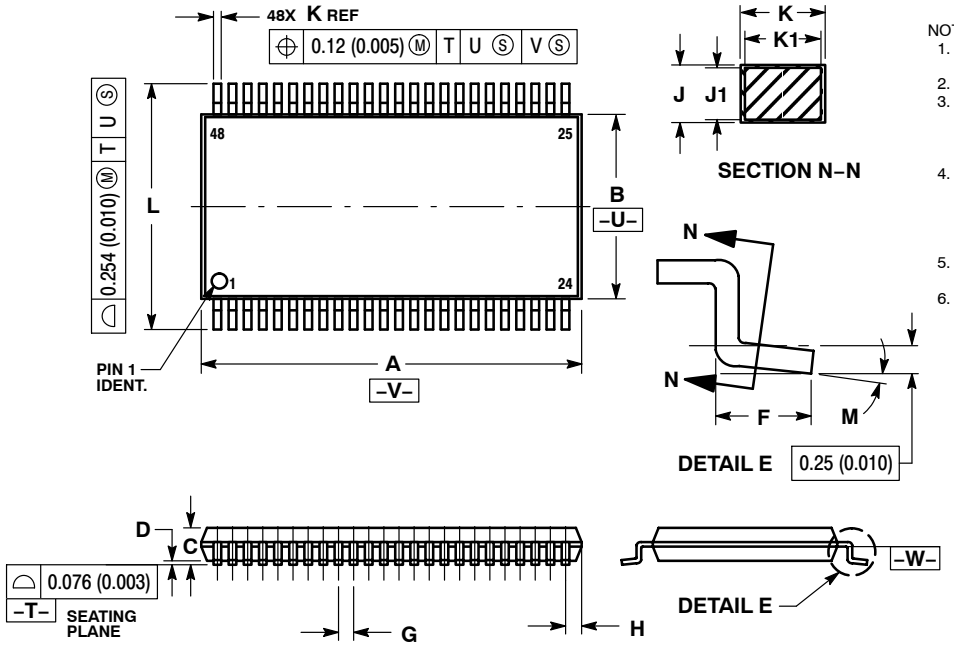
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

1

SCALE 1:1

TSSOP−48
CASE 1201
ISSUE B

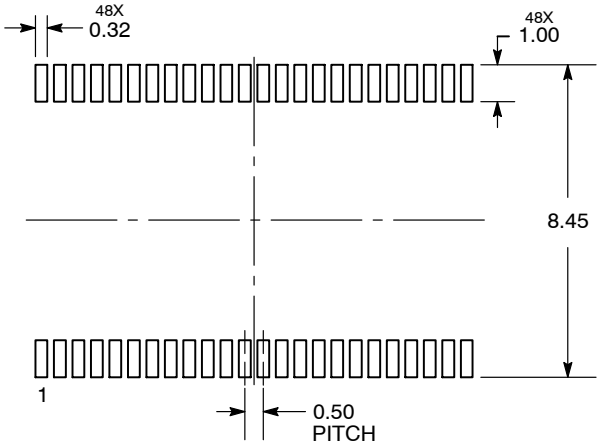
DATE 06 JUL 2010



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	−−−	1.10	−−−	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	−−−	0.015	−−−
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−48**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales