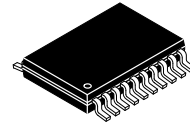


# 3.3V / 5V 1:5 Differential ECL/PECL/HSTL Clock Driver MC100EP14



TSSOP-20  
DT SUFFIX  
CASE 948E

## Description

The MC100EP14 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the  $V_{BB}$  output is used). HSTL inputs can be used when the LVEP14 is operating under PECL conditions.

The EP14 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

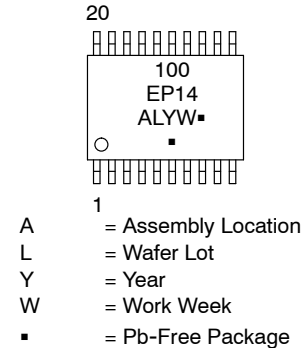
The common enable ( $\overline{EN}$ ) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

## Features

- 400 ps Typical Propagation Delay
- 100 ps Device-to-Device Skew
- 25 ps Within Device Skew
- Maximum Frequency > 2 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode:  
 $V_{CC} = 3.0$  V to 5.5 V with  $V_{EE} = 0$  V
- NECL Mode:  
 $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-5.5$  V
- Open Input Default State
- These are Pb-Free Devices

## MARKING DIAGRAM\*



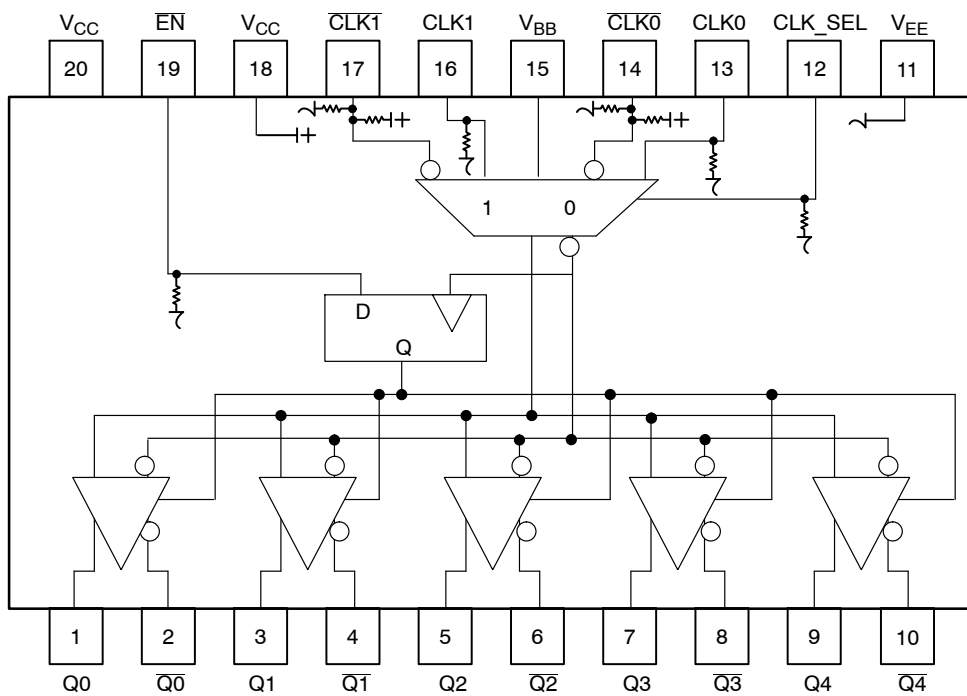
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC100EP14



**WARNING:** All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

### Figure 1. TSSOP-20 (Top View) and Logic Diagram

### Table 1. PIN DESCRIPTION

| Pin             | Function                           |
|-----------------|------------------------------------|
| CLK0*, CLK0**   | ECL/PECL/HSTL CLK Input            |
| CLK1*, CLK1**   | ECL/PECL/HSTL CLK Input            |
| Q0:4, Q0:4      | ECL/PECL Outputs                   |
| CLK_SEL*        | ECL/PECL Active Clock Select Input |
| EN*             | ECL Sync Enable                    |
| V <sub>BB</sub> | Reference Voltage Output           |
| V <sub>CC</sub> | Positive Supply                    |
| V <sub>EE</sub> | Negative Supply                    |

\* Pins will default low when left open.

\*\* Pins will default to  $V_{CC}/2$  when left open.

### Table 2. FUNCTION TABLE

| CLK0 | CLK1 | CLK_SEL | EN | Q  |
|------|------|---------|----|----|
| L    | X    | L       | L  | L  |
| H    | X    | L       | L  | H  |
| X    | L    | H       | L  | L  |
| X    | H    | H       | L  | H  |
| X    | X    | X       | H  | L* |

\* On next negative transition of CLK0 or CLK1

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**Table 3. ATTRIBUTES**

| Characteristics                                               | Value                                                     |                             |
|---------------------------------------------------------------|-----------------------------------------------------------|-----------------------------|
| Internal Input Pulldown Resistor                              | 75 kΩ                                                     |                             |
| Internal Input Pullup Resistor                                | 37.5 kΩ                                                   |                             |
| ESD Protection                                                | Human Body Model<br>Machine Model<br>Charged Device Model | > 4 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb Pkg                                                    | Pb-Free Pkg                 |
| TSSOP-8                                                       | Level 1                                                   | Level 1                     |
| Flammability Rating                                           | Oxygen Index: 28 to 34                                    | UL 94 V-0 @ 0.125 in        |
| Transistor Count                                              | 357 Devices                                               |                             |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |                                                           |                             |

1. For additional information, see Application Note [AND8003/D](#).

**Table 4. MAXIMUM RATINGS**

| Symbol           | Parameter                                          | Condition 1                                    | Condition 2                                                          | Rating      | Unit         |
|------------------|----------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------|-------------|--------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |                                                                      | 6           | V            |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |                                                                      | -6          | V            |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>-6     | V<br>V       |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |                                                                      | 50<br>100   | mA<br>mA     |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source                        |                                                |                                                                      | ± 0.5       | mA           |
| T <sub>A</sub>   | Operating Temperature Range                        |                                                |                                                                      | -40 to +85  | °C           |
| T <sub>stg</sub> | Storage Temperature Range                          |                                                |                                                                      | -65 to +150 | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP-20<br>TSSOP-20                                                 | 140<br>100  | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | TSSOP-20                                                             | 23 to 41    | °C/W         |
| T <sub>sol</sub> | Wave Solder                                        | <2 to 3 sec @ 248 °C                           |                                                                      | 265         | °C           |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



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**Table 5. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2)

| Symbol      | Characteristic                                                             | -40°C                                     |      |      | 25°C        |      |      | 85°C        |      |      | Unit          |
|-------------|----------------------------------------------------------------------------|-------------------------------------------|------|------|-------------|------|------|-------------|------|------|---------------|
|             |                                                                            | Min                                       | Typ  | Max  | Min         | Typ  | Max  | Min         | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                       | 45                                        | 55   | 65   | 48          | 58   | 68   | 52          | 62   | 72   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 3)                                               | 2155                                      | 2280 | 2405 | 2155        | 2280 | 2405 | 2155        | 2280 | 2405 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 3)                                                | 1305                                      | 1480 | 1605 | 1305        | 1480 | 1605 | 1305        | 1480 | 1605 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                          | 2075                                      |      | 2420 | 2075        |      | 2420 | 2075        |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                           | 1305                                      |      | 1675 | 1305        |      | 1675 | 1305        |      | 1675 | mV            |
| $V_{BB}$    | Output Voltage Reference                                                   | 1775                                      | 1875 | 1975 | 1775        | 1875 | 1975 | 1775        | 1875 | 1975 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.2                                       |      | 3.3  | 1.2         |      | 3.3  | 1.2         |      | 3.3  | V             |
| $I_{IH}$    | Input HIGH Current                                                         |                                           |      | 150  |             |      | 150  |             |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                          | $\overline{D}$ 0.5<br>$\overline{D}$ -150 |      |      | 0.5<br>-150 |      |      | 0.5<br>-150 |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

3. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

4.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 6. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 5)

| Symbol      | Characteristic                                                             | -40°C                                     |      |      | 25°C        |      |      | 85°C        |      |      | Unit          |
|-------------|----------------------------------------------------------------------------|-------------------------------------------|------|------|-------------|------|------|-------------|------|------|---------------|
|             |                                                                            | Min                                       | Typ  | Max  | Min         | Typ  | Max  | Min         | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                       | 45                                        | 55   | 65   | 48          | 58   | 68   | 52          | 62   | 72   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 6)                                               | 3855                                      | 3980 | 4105 | 3855        | 3980 | 4105 | 3855        | 3980 | 4105 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 6)                                                | 3005                                      | 3180 | 3305 | 3005        | 3180 | 3305 | 3005        | 3180 | 3305 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                          | 3775                                      |      | 4120 | 3775        |      | 4120 | 3775        |      | 4120 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                           | 3005                                      |      | 3375 | 3005        |      | 3375 | 3005        |      | 3375 | mV            |
| $V_{BB}$    | Output Voltage Reference                                                   | 3475                                      | 3575 | 3675 | 3475        | 3575 | 3675 | 3475        | 3575 | 3675 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | 1.2                                       |      | 5.0  | 1.2         |      | 5.0  | 1.2         |      | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current                                                         |                                           |      | 150  |             |      | 150  |             |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                          | $\overline{D}$ 0.5<br>$\overline{D}$ -150 |      |      | 0.5<br>-150 |      |      | 0.5<br>-150 |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

6. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 7. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 8)

| Symbol      | Characteristic                                                              | -40°C        |       |       | 25°C         |       |       | 85°C         |       |       | Unit          |
|-------------|-----------------------------------------------------------------------------|--------------|-------|-------|--------------|-------|-------|--------------|-------|-------|---------------|
|             |                                                                             | Min          | Typ   | Max   | Min          | Typ   | Max   | Min          | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                                        | 45           | 55    | 65    | 48           | 58    | 68    | 52           | 62    | 72    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 9)                                                | -1145        | -1020 | -895  | -1145        | -1020 | -895  | -1145        | -1020 | -895  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 9)                                                 | -1995        | -1820 | -1695 | -1995        | -1820 | -1695 | -1995        | -1820 | -1695 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                           | -1225        |       | -880  | -1225        |       | -880  | -1225        |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                            | -1995        |       | -1625 | -1995        |       | -1625 | -1995        |       | -1625 | mV            |
| $V_{BB}$    | Output Reference Voltage                                                    | -1525        | -1425 | -1325 | -1525        | -1425 | -1325 | -1525        | -1425 | -1325 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10) | $V_{EE}+1.2$ |       | 0.0   | $V_{EE}+1.2$ |       | 0.0   | $V_{EE}+1.2$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current                                                          |              |       | 150   |              |       | 150   |              |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current CLK<br>CLK                                                | 0.5<br>-150  |       |       | 0.5<br>-150  |       |       | 0.5<br>-150  |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Input and output parameters vary 1:1 with  $V_{CC}$ .

9. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

10.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 8. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 11)

| Symbol                 | Characteristic                                                               | -40°C      |           |           | 25°C       |           |           | 85°C       |           |           | Unit |
|------------------------|------------------------------------------------------------------------------|------------|-----------|-----------|------------|-----------|-----------|------------|-----------|-----------|------|
|                        |                                                                              | Min        | Typ       | Max       | Min        | Typ       | Max       | Min        | Typ       | Max       |      |
| $V_{OPP}$              | Output Voltage Amplitude @ 2 GHz (Figure 2)                                  | 440        | 540       |           | 420        | 520       |           | 380        | 480       |           | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output Differential                                     | 275        | 330       | 400       | 275        | 375       | 450       | 280        | 380       | 480       | ps   |
| $t_{skew}$             | Within-Device Skew<br>Device-to-Device Skew (Note 12)                        |            | 25<br>100 | 35<br>125 |            | 30<br>150 | 45<br>175 |            | 40<br>175 | 50<br>200 | ps   |
| $t_s$<br>$t_h$         | Setup Time to CLK $\overline{EN}$ to CLK<br>Hold Time $\overline{EN}$ to CLK | 100<br>200 | 50<br>140 |           | 100<br>200 | 50<br>140 |           | 100<br>200 | 50<br>140 |           | ps   |
| $t_{JITTER}$           | Cycle-to-Cycle Jitter (Figure 2)                                             |            | 0.2       | < 1       |            | 0.2       | < 1       |            | 0.2       | < 1       | ps   |
| $V_{PP}$               | Minimum Input Swing                                                          | 150        | 800       | 1200      | 150        | 800       | 1200      | 150        | 800       | 1200      | mV   |
| $t_r/t_f$              | Output Rise/Fall Time (20%–80%)                                              | 105        | 155       | 205       | 145        | 200       | 270       | 150        | 225       | 300       | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

12. Skew is measured between outputs under identical transitions.



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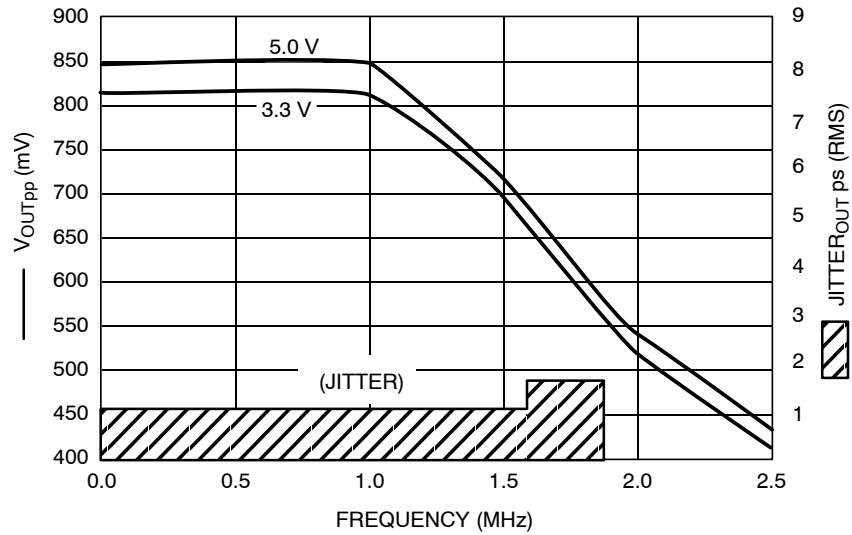


Figure 2.  $F_{max}$ /Jitter

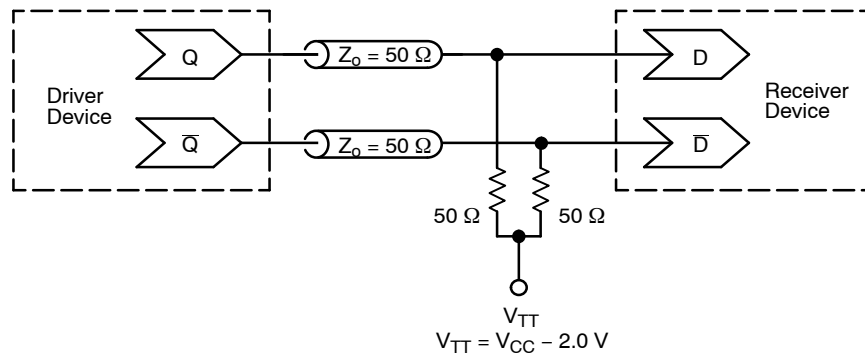


Figure 3. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

| Device         | Package               | Shipping <sup>†</sup> |
|----------------|-----------------------|-----------------------|
| MC100EP14DTG   | TSSOP-20<br>(Pb-Free) | 75 Units / Rail       |
| MC100EP14DTR2G | TSSOP-20<br>(Pb-Free) | 2500 / Tape & Rail    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#)

## MC100EP14

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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## MC100EP14

### REVISION HISTORY

| Revision | Description of Changes                           | Date     |
|----------|--------------------------------------------------|----------|
| 8        | Rebranded the Data Sheet to <b>onsemi</b> format | 7/9/2025 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



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