

High-Current, High & Low-Side, Gate-Drive IC

FAN7390

Description

The FAN7390 is a monolithic high- and low-side gate-drive IC, which can drive high speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

onsemi's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level shift circuit offers high-side gate driver operation up to $V_S = -9.8$ V (typical) for $V_{BS} = 15$ V.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low output voltage drop feature make this device suitable for the PDP sustain pulse driver, motor driver, switching power supply, and high-power DC-DC converter applications.

Features

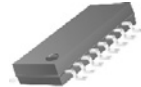
- Floating Channels for Bootstrap Operation to +600 V
- Typically 4.5 A / 4.5 A Sourcing / Sinking Current Driving Capability
- Common-Mode dv/dt Noise-Canceling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- Logic (V_{SS}) and Power (COM) Ground ± 7 V Offset
- 3.3 V and 5 V Input Logic Compatible
- Output In-Phase with Input
- This is a Pb-Free Device

Applications

- PDP Sustain Driver
- HID Lamp Ballast
- SMPS
- Motor Driver

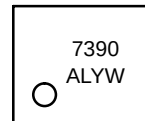


SOIC8
8-SOP
CASE 751EG



SOIC14
14-SOP
CASE 751ER

MARKING DIAGRAM



FAN7390MX



FAN7390M1X

7390, = Device Code
FAN7390

A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week
&Z = Assembly Plant Code
&3 = 3-Digit Date Code
&K = 2-Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 12.

FAN7390

TYPICAL APPLICATION CIRCUIT

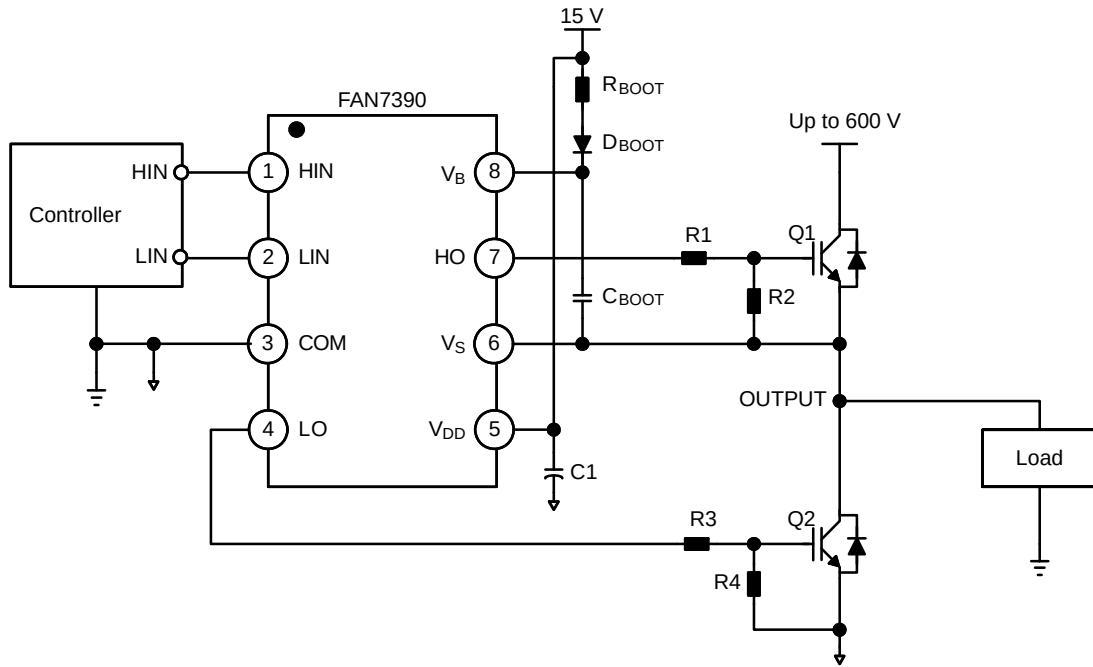


Figure 1. Application Circuit for Half-Bridge (Referenced 8-SOP)

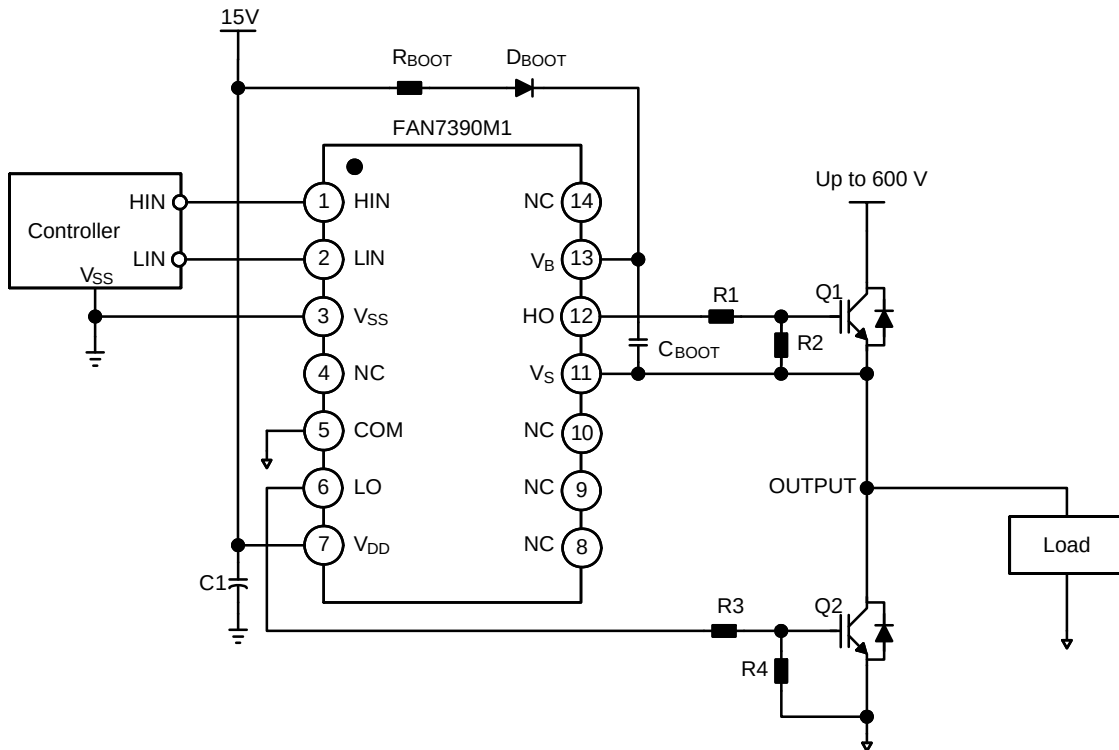


Figure 2. Application Circuit for Half-Bridge (Referenced 14-SOP)

FAN7390

INTERNAL BLOCK DIAGRAM

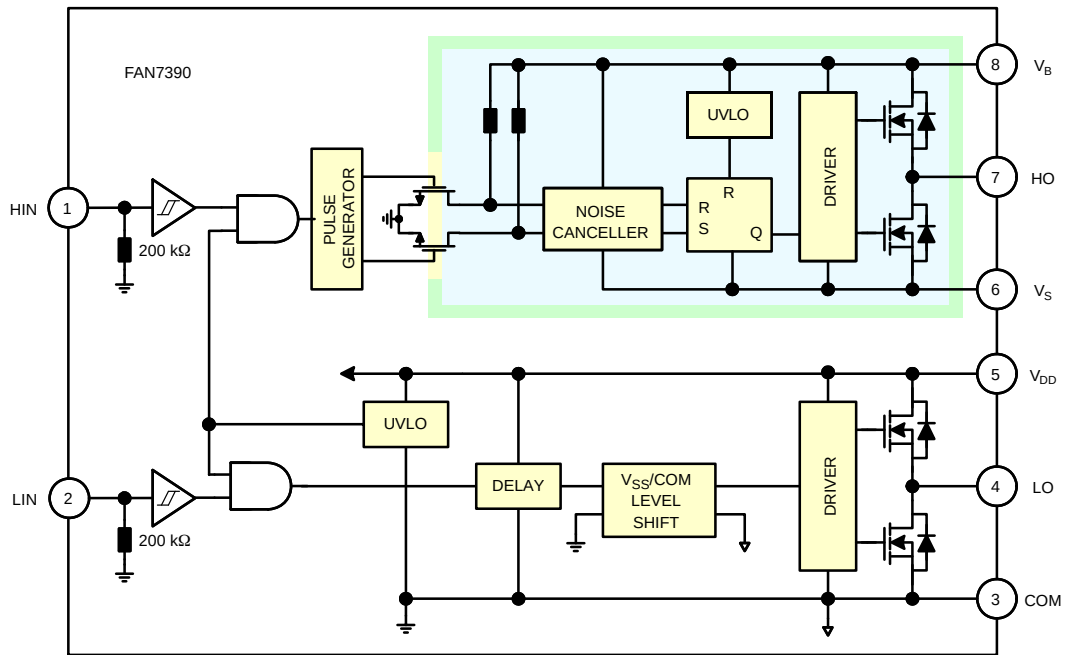


Figure 3. Functional Block Diagram (Referenced 8-SOP)

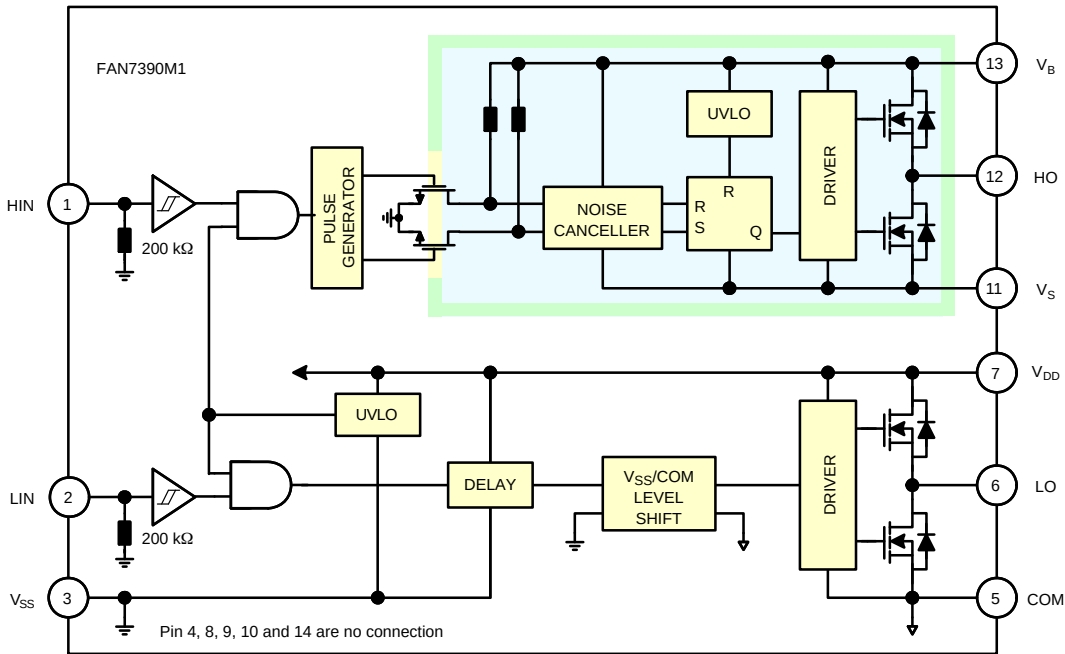


Figure 4. Functional Block Diagram (Referenced 14-SOP)

FAN7390

PIN CONFIGURATION

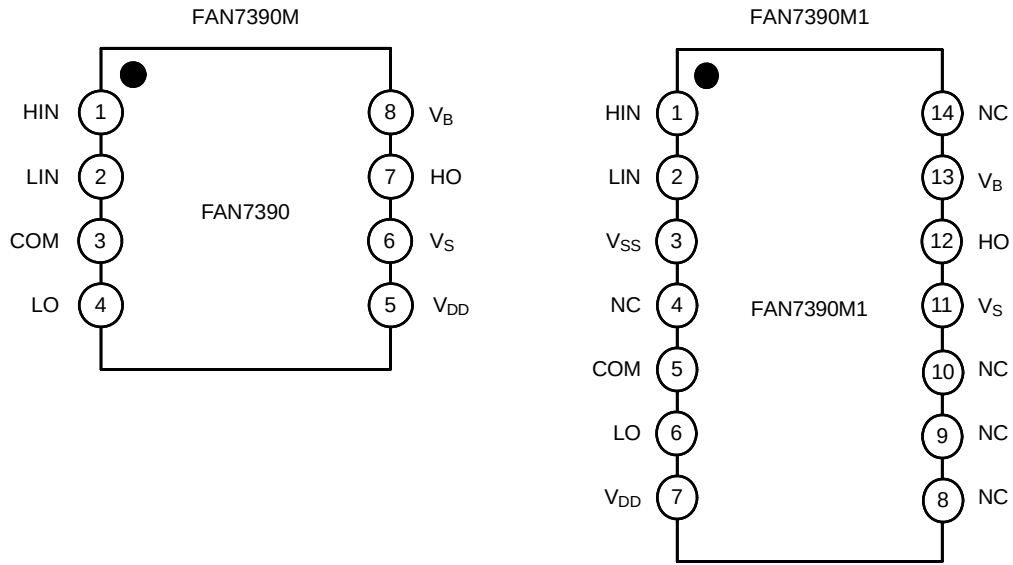


Figure 5. Pin Assignments (Top View)

PIN DEFINITIONS

8-Pin	14-Pin	Name	Description
1	1	HIN	Logic Input for High-Side Gate Driver Output
2	2	LIN	Logic Input for Low-Side Gate Driver Output
	3	V _{SS}	Logic Ground (FAN7390M1 only)
3	5	COM	Low-Side Driver Return
4	6	LO	Low-Side Driver Output
5	7	V _{DD}	Low-Side and Logic Part Supply Voltage
6	11	V _S	High-Voltage Floating Supply Return
7	12	HO	High-Side Driver Output
8	13	V _B	High-Side Floating Supply
	4, 8, 9, 10, 14	NC	No Connect

FAN7390

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Symbol	Characteristics	Min	Max	Unit
V _S	High-Side Floating Supply Offset Voltage	V _B – 25	V _B + 0.3	V
V _B	High-Side Floating Supply Voltage	–0.3	625.0	V
V _{HO}	High-Side Floating Output Voltage HO	V _S – 0.3	V _B + 0.3	V
V _{DD}	Low-Side and Logic Fixed Supply Voltage	–0.3	25.0	V
V _{LO}	Low-Side Output Voltage LO	–0.3	V _{DD} + 0.3	V
V _{IN}	Logic Input Voltage (HIN and LIN)	V _{SS} – 0.3	V _{DD} + 0.3	V
V _{SS}	Logic Ground (FAN7390M1 only)	V _{DD} – 25	V _{DD} + 0.3	V
dV _S /dt	Allowable Offset Voltage Slew Rate	–	50	V/ns
P _D (Note 1, 2, 3)	Power Dissipation	8-SOP	0.625	W
		14-SOP	1.000	
θ _{JA}	Thermal Resistance, Junction-to-Ambient	8-SOP	200	°C/W
		14-SOP	110	
T _J	Junction Temperature	–	+150	°C
T _{STG}	Storage Temperature	–	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
JESD51-2: Integral circuits thermal test method environmental conditions – natural convection
JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
3. Do not exceed P_D under any circumstances.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _B	High-Side Floating Supply Voltage	V _S + 10	V _S + 22	V
V _S	High-Side Floating Supply Offset Voltage	6 – V _{DD}	600	V
V _{HO}	High-Side Output Voltage	V _S	V _B	V
V _{DD}	Low-Side and Logic Supply Voltage	10	22	V
V _{LO}	Low-Side Output Voltage	COM	V _{DD}	V
V _{IN}	Logic Input Voltage (HIN and LIN)	V _{SS}	V _{DD}	V
T _A	Operating Ambient Temperature	–40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.



ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD} , V_{BS}) = 15.0 V, $V_S = V_{SS} = \text{COM}$, $T_A = 25^\circ\text{C}$, unless otherwise specified. The V_{IL} , V_{IH} , and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input signals HIN and LIN. The V_O and I_O parameters are referenced to COM and V_S is applicable to the respective output signals HO and LO.)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
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POWER SUPPLY SECTION (V_{DD} AND V_{BS})

V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} Supply Under-Voltage Positive-going Threshold		8.0	8.8	9.8	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} Supply Under-Voltage Negative-going Threshold		7.4	8.3	9.0	
V_{DDUVH} V_{BSUVH}	V_{DD} and V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage		–	0.5	–	
I_{LK}	Offset Supply Leakage Current	$V_B = V_S = 600\text{ V}$	–	–	50	μA
I_{QBS}	Quiescent V_{BS} Supply Current	$V_{IN} = 0\text{ V or } 5\text{ V}$	–	45	80	
I_{QDD}	Quiescent V_{DD} Supply Current	$V_{IN} = 0\text{ V or } 5\text{ V}$	–	75	110	
I_{PBS}	Operating V_{BS} Supply Current	$f_{IN} = 20\text{ kHz, rms value}$	–	530	640	μA
I_{PDD}	Operating V_{DD} Supply Current	$f_{IN} = 20\text{ kHz, rms value}$	–	530	640	

LOGIC INPUT SECTION (HIN, LIN)

V_{IH}	Logic “1” Input Voltage		2.5	–	–	V
V_{IL}	Logic “0” Input Voltage		–	–	1.2	
I_{IN+}	Logic “1” Input Bias Current	$V_{IN} = 5\text{ V}$	–	25	50	μA
I_{IN-}	Logic “0” Input Bias Current	$V_{IN} = 0\text{ V}$	–	1.0	2.0	
R_{IN}	Input Pull-down Resistance		100	200	–	k Ω

GATE DRIVER OUTPUT SECTION (HO, LO)

V_{OH}	High-level Output Voltage, $V_{BIAS}-V_O$	No Load	–	–	1.0	V
V_{OL}	Low-level Output Voltage, V_O	No Load	–	–	35	mV
I_{O+}	Output High, Short-circuit Pulsed Current (Note 4)	$V_O = 0\text{ V}$, $V_{IN} = 5\text{ V}$ with $PW < 10\text{ }\mu\text{s}$	3.5	4.5		A
I_{O-}	Output Low, Short-circuit Pulsed Current (Note 4)	$V_O = 15\text{ V}$, $V_{IN} = 0\text{ V}$ with $PW < 10\text{ }\mu\text{s}$	3.5	4.5	–	
V_S	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO		–	–9.8	–7.0	V
$V_{SS}-\text{COM}$	$V_{SS}-\text{COM}/\text{COM}-V_{SS}$ Voltage Endurability		–7.0	–	7.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. This parameter guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD} , V_{BS}) = 15.0 V, $V_S = V_{SS} = \text{COM} = 0\text{ V}$, $C_L = 1000\text{ pF}$, and $T_A = 25^\circ\text{C}$ unless otherwise specified.)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
t_{on}	Turn-on Propagation Delay	$V_S = 0\text{ V}$	–	140	220	ns
t_{off}	Turn-off Propagation Delay	$V_S = 0\text{ V}$	–	140	220	
MT	Delay Matching, HS & LS Turn-on/off		–	0	50	
t_r	Turn-on Rise Time		–	25	50	
t_f	Turn-off Fall Time		–	20	45	

TYPICAL CHARACTERISTICS

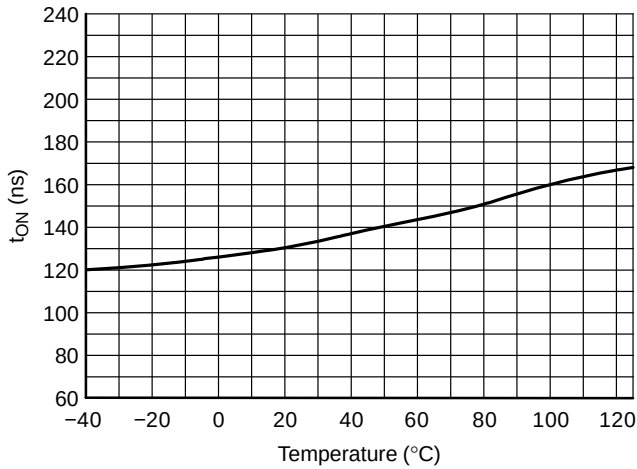


Figure 6. Turn-on Propagation Delay vs. Temperature

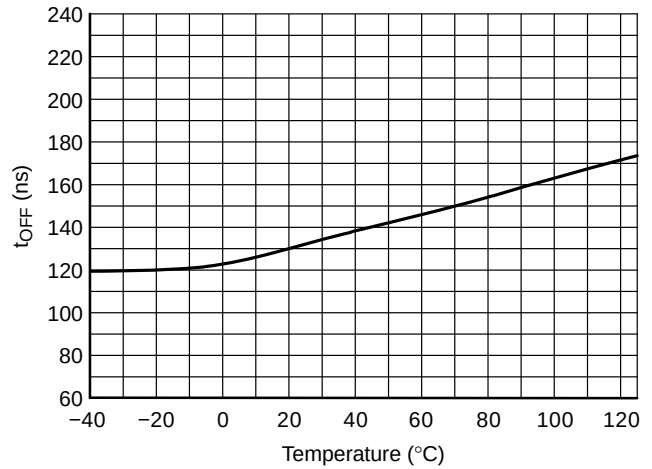


Figure 7. Turn-off Propagation Delay vs. Temperature

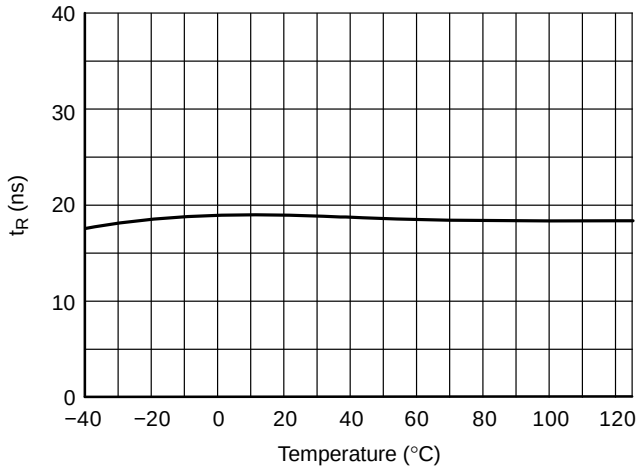


Figure 8. Turn-on Rise Time vs. Temperature

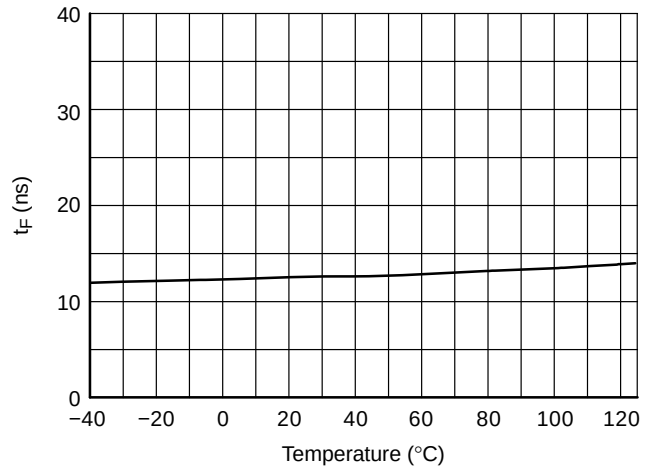


Figure 9. Turn-off Fall Time vs. Temperature

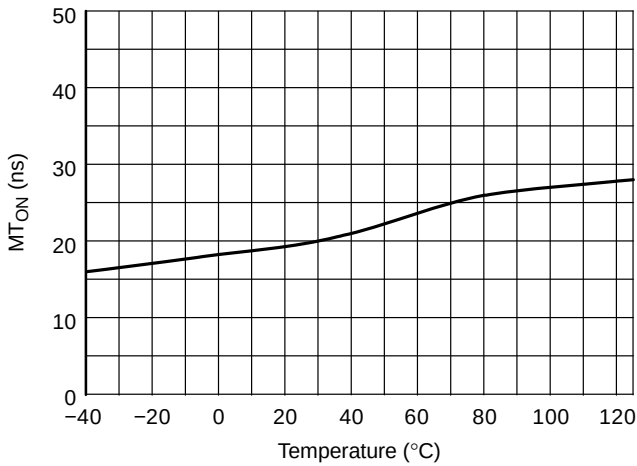


Figure 10. Turn-on Delay Matching vs. Temperature

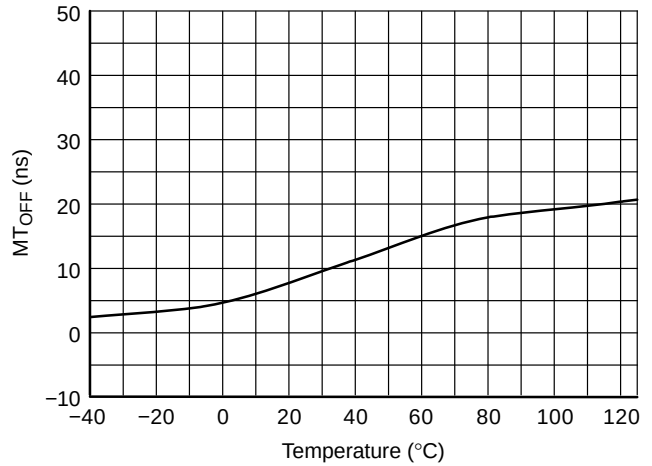


Figure 11. Turn-off Delay Matching vs. Temperature

TYPICAL CHARACTERISTICS (continued)

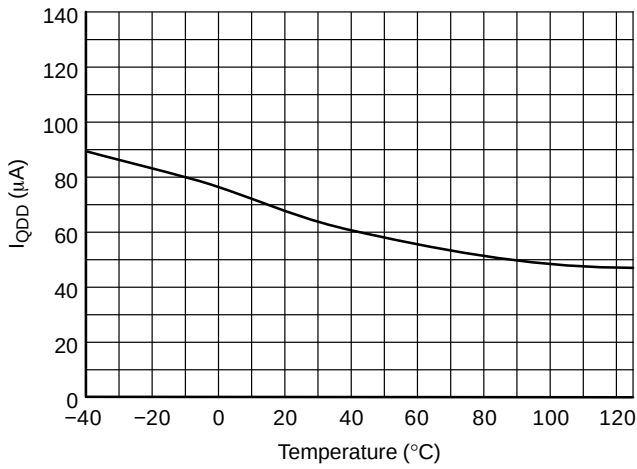


Figure 12. Quiescent V_{DD} Supply Current vs. Temperature

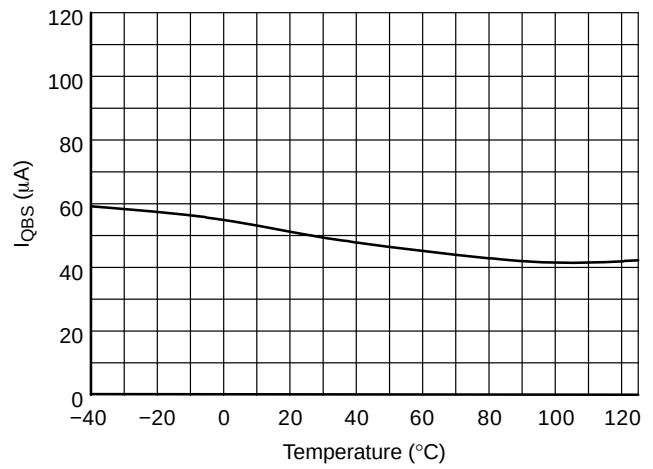


Figure 13. Quiescent V_{BS} Supply Current vs. Temperature

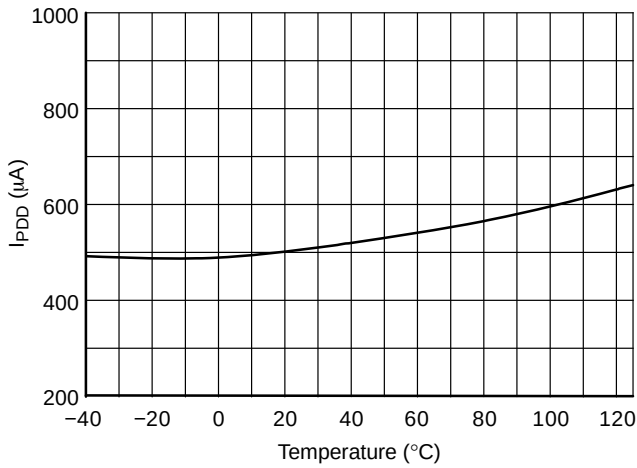


Figure 14. Operating V_{DD} Supply Current vs. Temperature

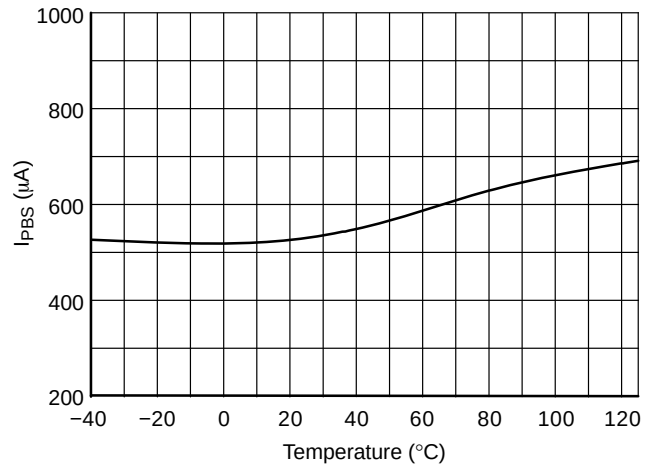


Figure 15. Operating V_{BS} Supply Current vs. Temperature

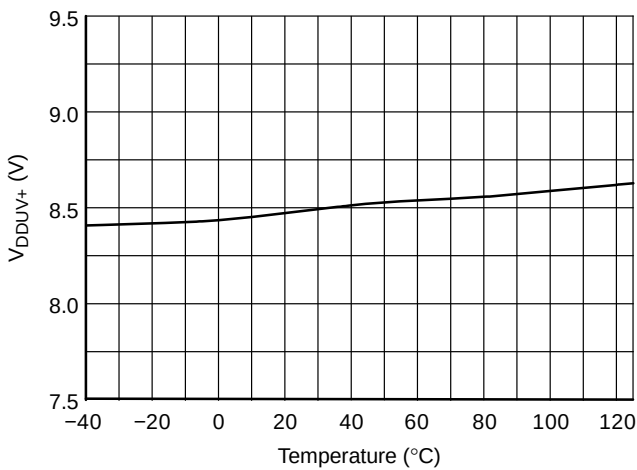


Figure 16. V_{DD} UVLO+ vs. Temperature

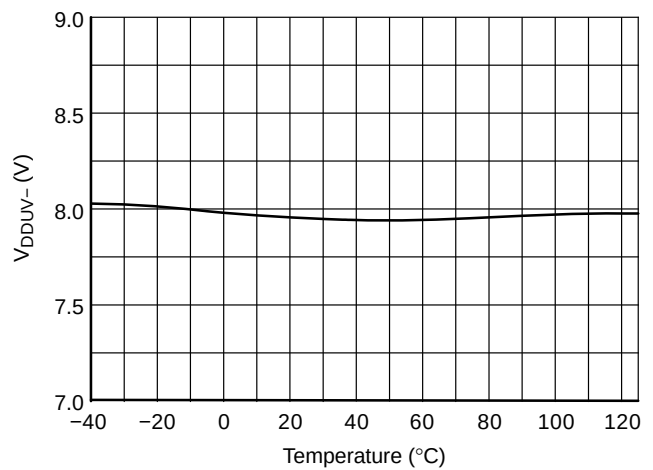


Figure 17. V_{DD} UVLO- vs. Temperature

TYPICAL CHARACTERISTICS (continued)

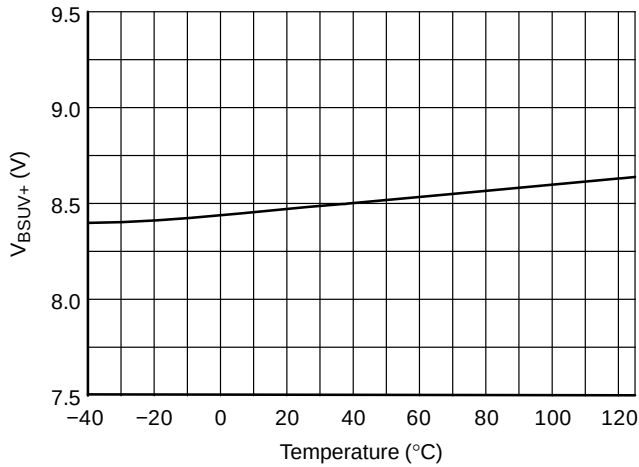


Figure 18. V_{BS} UVLO+ vs. Temperature

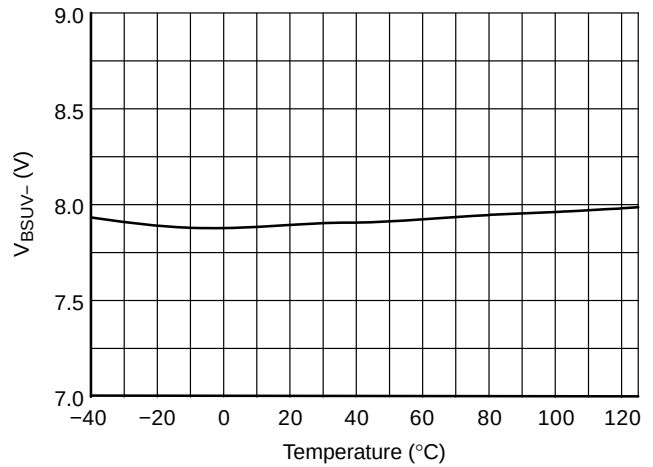


Figure 19. V_{BS} UVLO- vs. Temperature

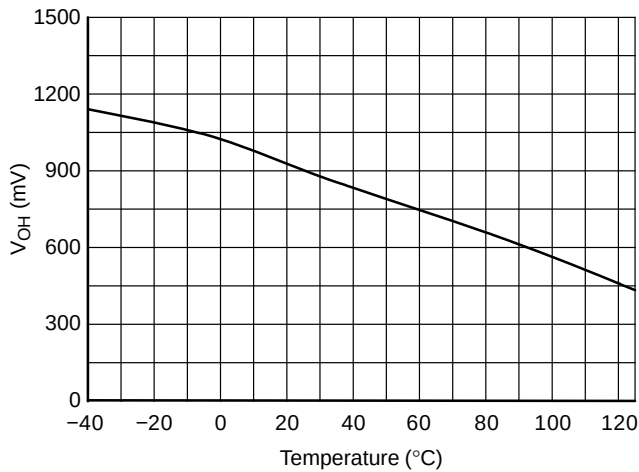


Figure 20. High-Level Output Voltage vs. Temperature

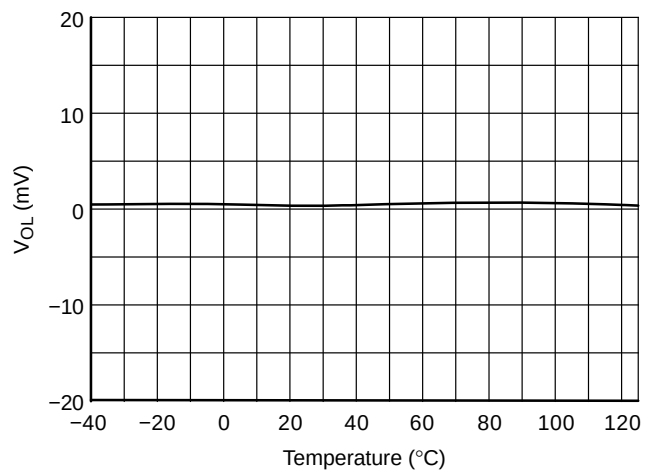


Figure 21. Low-Level Output Voltage vs. Temperature

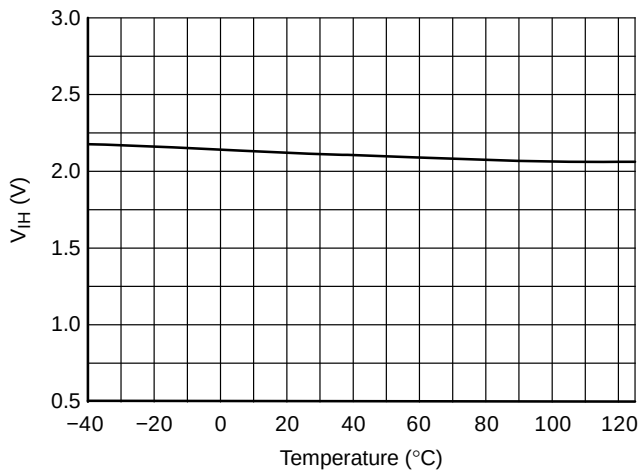


Figure 22. Logic High Input Voltage vs. Temperature

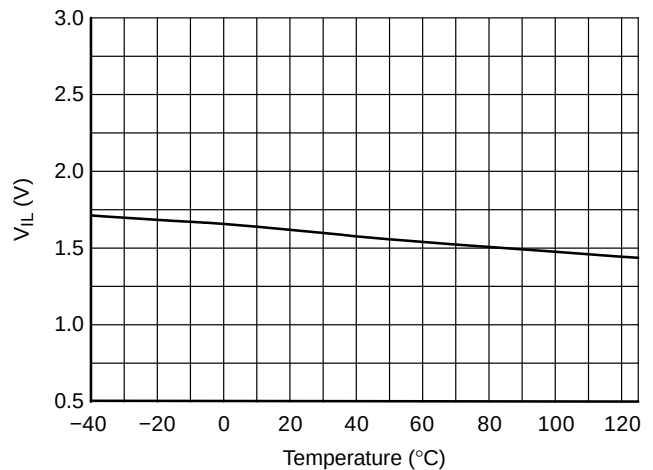


Figure 23. Low Input Voltage vs. Temperature

TYPICAL CHARACTERISTICS (continued)

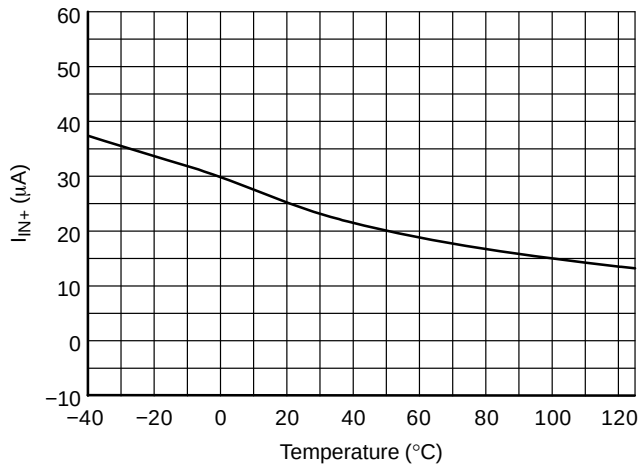


Figure 24. Logic Input High Bias Current vs. Temperature

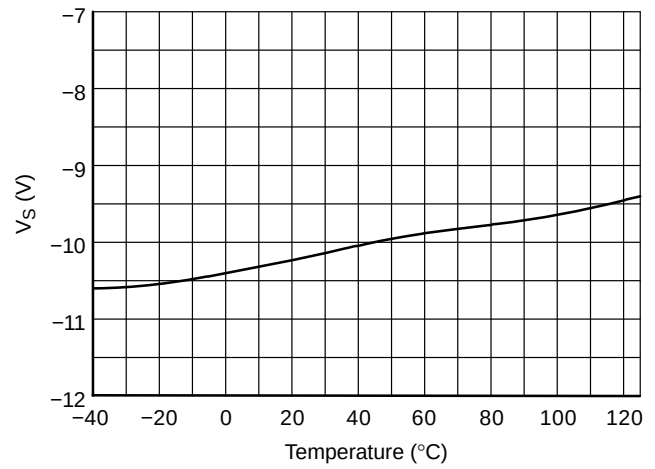


Figure 25. Allowable Negative V_S Voltage vs. Temperature

SWITCHING TIME DEFINITIONS

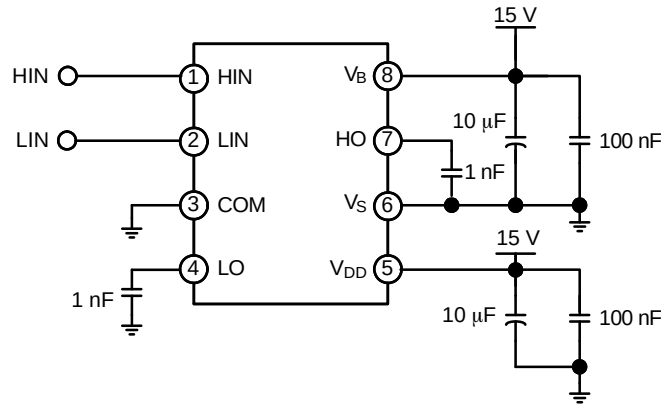


Figure 26. Switching Time Test Circuit (Referenced 8-SOP)

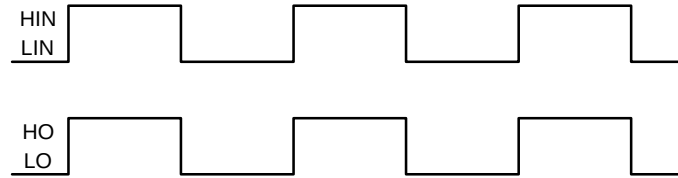


Figure 27. Input/Output Timing Diagram

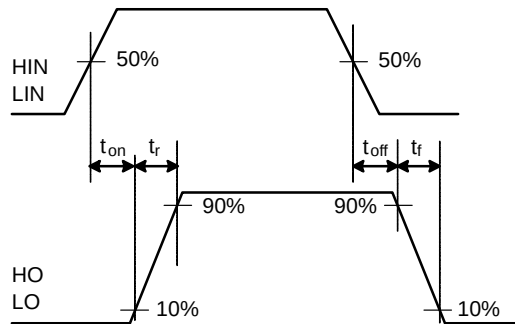


Figure 28. Switching Time Waveform Definitions

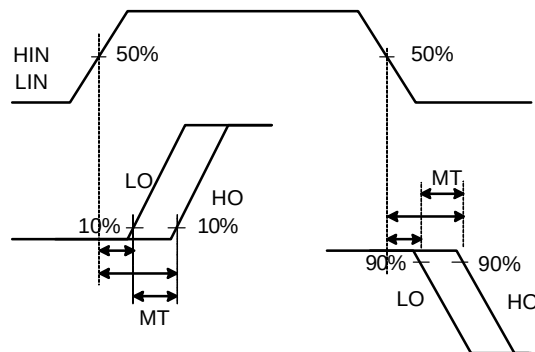


Figure 29. Delay Matching Waveform Definitions

FAN7390

ORDERING INFORMATION

Device	Package	Operating Temperature Range	Shipping [†]
FAN7390MX	SOIC8 8-SOP (Pb-Free)	-40 °C~125 °C	3000 / Tape & Reel

DISCONTINUED (Note 5)

FAN7390M1X	SOIC14 14-SOP (Pb-Free)	-40 °C~125 °C	3000 / Tape & Reel
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[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

5. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



FAN7390

REVISION HISTORY

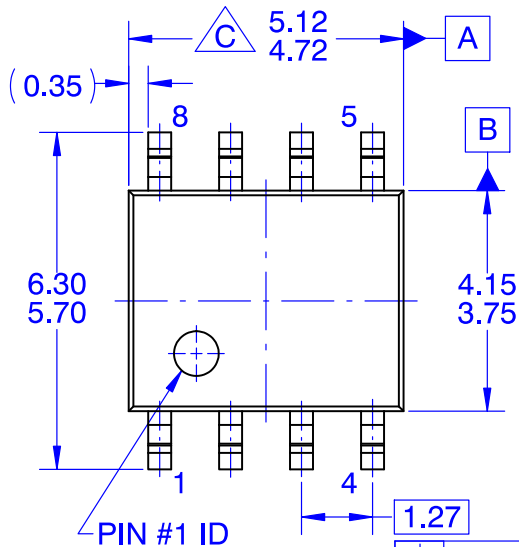
Revision	Description of Changes	Date
3	Rebranded the document to onsemi format. FAN7390M1X OPN marked as Discontinued.	3/11/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

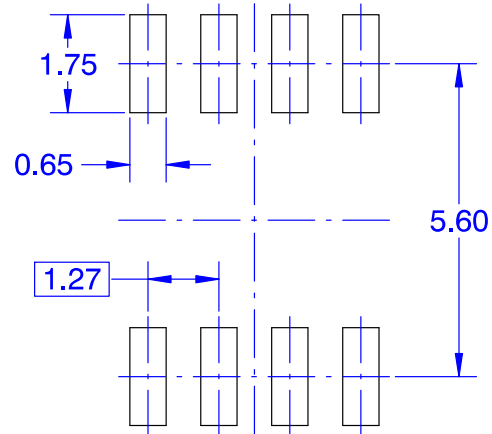


SOIC8
CASE 751EG
ISSUE O

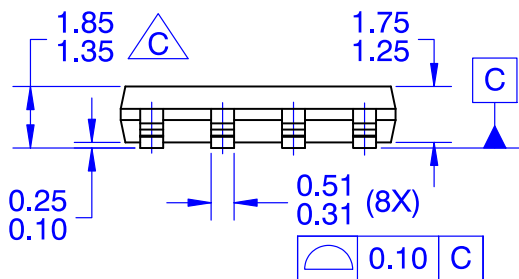
DATE 30 SEP 2016



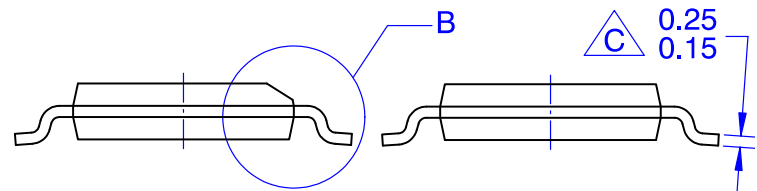
TOP VIEW



LAND PATTERN RECOMMENDATION



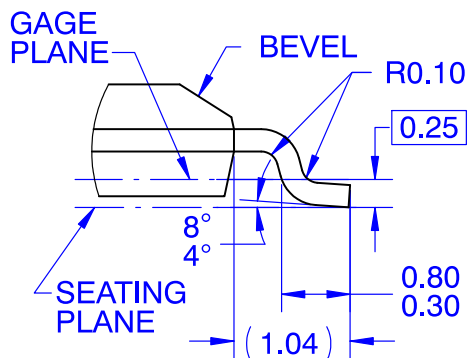
FRONT VIEW



OPTION A
BEVEL EDGE

OPTION B
NON-BEVEL EDGE

SIDE VIEW



DETAIL "B"
SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

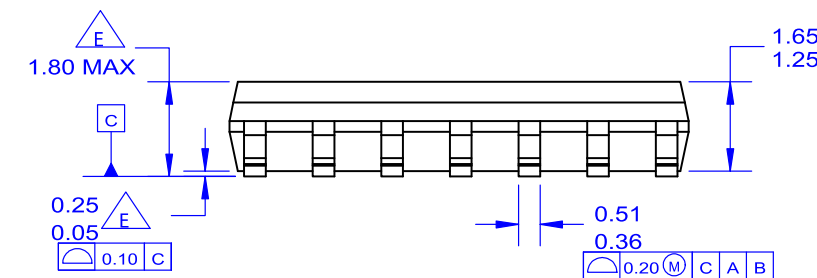
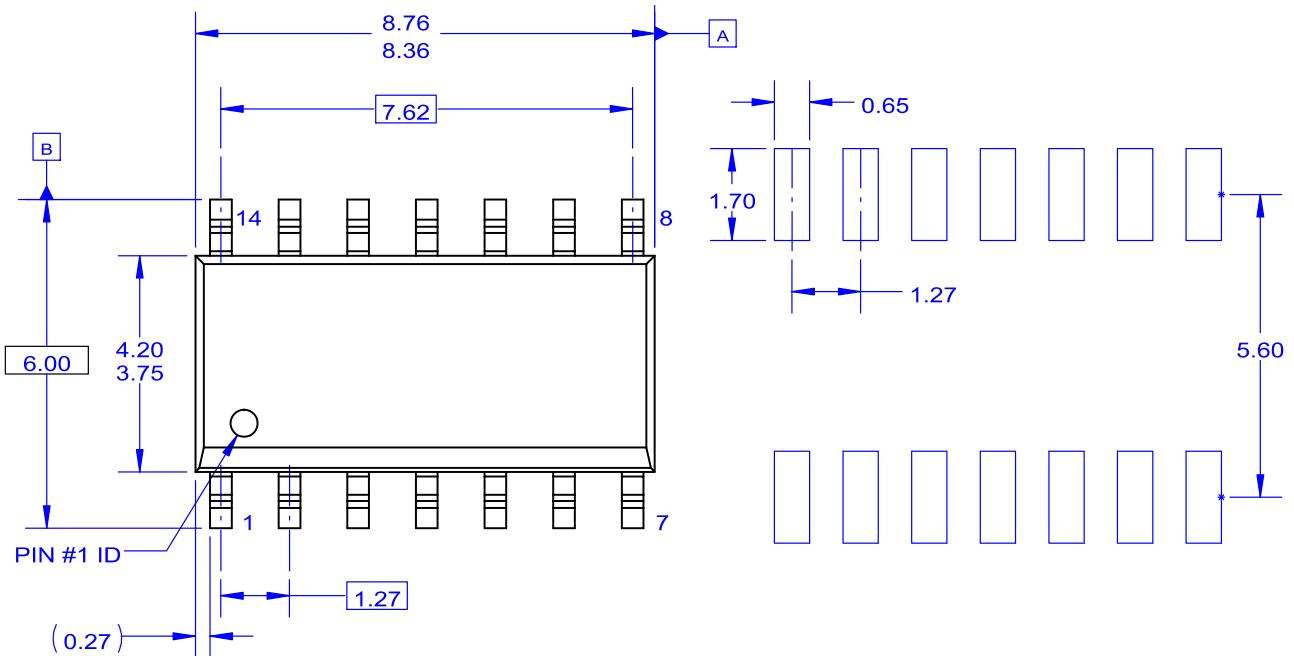
- A. THIS PACKAGE CONFORMS TO JEDEC MS-012 VARIATION A EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. OUT OF JEDEC STANDARD VALUE
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- E. LAND PATTERN AS PER IPC SOIC127P600X175-8M

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DESCRIPTION:	SOIC8	PAGE 1 OF 1

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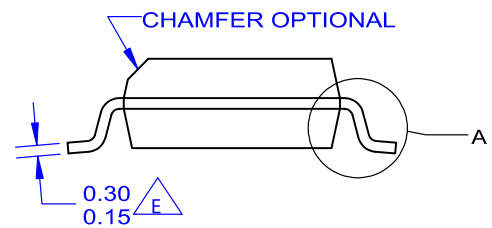
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ISSUE O

DATE 31 DEC 2016



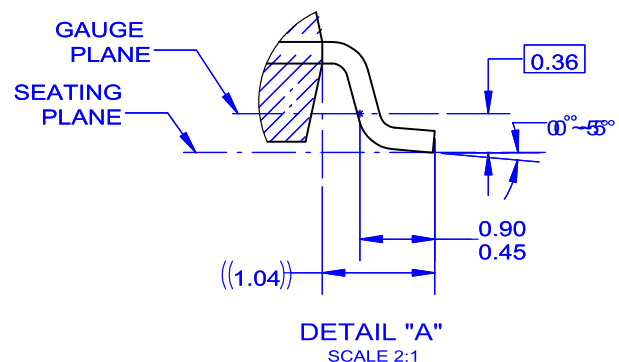
ALL LEAD TIPS

SIDE VIEW



NOTES: UNLESS OTHERWISE SPECIFIED

- A. THIS PACKAGE REFERENCE TO JEDEC MS-012 VARIATION AB.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
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