

# 128 Kb I<sup>2</sup>C CMOS Serial EEPROM with Software Write Protect

## CAT24S128

### Description

The CAT24S128 is a 128 Kb Serial CMOS EEPROM, internally organized as 16,384 words of 8 bits each.

It features a 64-byte page write buffer and supports both the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I<sup>2</sup>C protocol.

The device features programmable software write protection which provides partial as well as full memory array protection.

### Features

- Supports Standard, Fast and Fast-Plus I<sup>2</sup>C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 64-Byte Page Write Buffer
- User Programmable Block Write Protection – Protect 1/4, 1/2, 3/4 or Entire EEPROM Array
- Schmitt Triggers and Noise Suppression Filters on I<sup>2</sup>C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 40 Year Data Retention
- Industrial Temperature Range: –40 °C to +85 °C
- Ultra-thin 4-ball WLCSP Package
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant\*\*

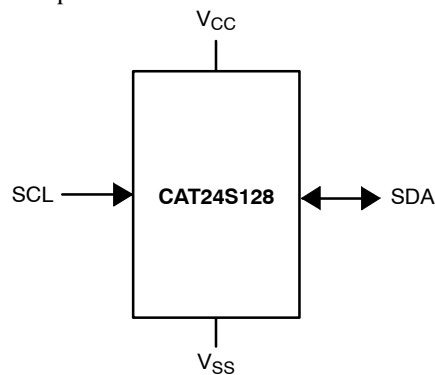


Figure 1. Functional Symbol

\* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, [SOLDERM/D](#).

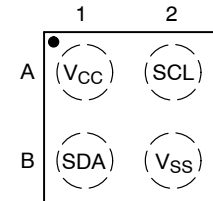


WLCSP-4  
C4A SUFFIX  
CASE 567KV



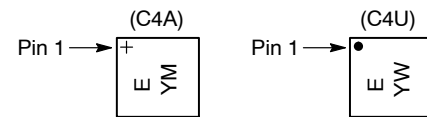
WLCSP-4  
C4U SUFFIX  
CASE 567PC

### PIN CONFIGURATION



WLCSP-4 (C4A, C4U)  
(Top View)

### MARKING DIAGRAMS



E = Specific Device Code  
(see ordering information)  
Y = Production Year (Last Digit)  
M = Production Month (1–9, O, N, D)  
W = Production Week Code

### PIN FUNCTION

| Pin Name        | Function                 |
|-----------------|--------------------------|
| SDA             | Serial Data Input/Output |
| SCL             | Serial Clock Input       |
| V <sub>CC</sub> | Power Supply             |
| V <sub>SS</sub> | Ground                   |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter                                          | Rating       | Unit |
|----------------------------------------------------|--------------|------|
| Storage Temperature                                | -65 to +150  | °C   |
| Voltage on Any Pin with Respect to Ground (Note 1) | -0.5 to +6.5 | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than -0.5 V or higher than  $V_{CC} + 1.0$  V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than  $V_{CC} + 1.5$  V, for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS** (Note 2)

| Symbol             | Parameter      | Min       | Unit                   |
|--------------------|----------------|-----------|------------------------|
| $N_{END}$ (Note 3) | Endurance      | 1,000,000 | Program / Erase Cycles |
| $T_{DR}$ (Note 4)  | Data Retention | 40        | Years                  |

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Page Mode,  $V_{CC} = 5$  V, 25 °C
4.  $T_A = 55$  °C

**Table 3. DC AND AC OPERATING CONDITIONS**

| Supply Voltage / Temperature Range                   | Operation    |
|------------------------------------------------------|--------------|
| $V_{CC} = 1.7$ V to 5.5 V / $T_A = -40$ °C to +85 °C | READ / WRITE |
| $V_{CC} = 1.6$ V to 5.5 V / $T_A = -40$ °C to +85 °C | READ         |
| $V_{CC} = 1.6$ V to 5.5 V / $T_A = 0$ °C to +85 °C   | WRITE        |

**Table 4. D.C. OPERATING CHARACTERISTICS**

| Symbol    | Parameter          | Test Conditions                        | Min                 | Max           | Unit    |
|-----------|--------------------|----------------------------------------|---------------------|---------------|---------|
| $I_{CCR}$ | Read Current       | Read, $f_{SCL} = 400$ kHz/1 MHz        |                     | 1             | mA      |
| $I_{CCW}$ | Write Current      |                                        |                     | 2             | mA      |
| $I_{SB}$  | Standby Current    | All I/O Pins at GND or $V_{CC}$        | $V_{CC} \leq 2.5$ V | 1             | $\mu$ A |
|           |                    |                                        | $V_{CC} > 2.5$ V    | 2             |         |
| $I_L$     | I/O Pin Leakage    | Pin at GND or $V_{CC}$                 |                     | 2             | $\mu$ A |
| $V_{IL1}$ | Input Low Voltage  | $V_{CC} \geq 2.5$ V                    | -0.5                | $0.3 V_{CC}$  | V       |
| $V_{IL2}$ | Input Low Voltage  | $V_{CC} < 2.5$ V                       | -0.5                | $0.25 V_{CC}$ | V       |
| $V_{IH1}$ | Input High Voltage | $V_{CC} \geq 2.5$ V                    | $0.7 V_{CC}$        | $V_{CC} + 1$  | V       |
| $V_{IH2}$ | Input High Voltage | $V_{CC} < 2.5$ V                       | $0.75 V_{CC}$       | $V_{CC} + 1$  | V       |
| $V_{OL1}$ | Output Low Voltage | $V_{CC} \geq 2.5$ V, $I_{OL} = 3.0$ mA |                     | 0.4           | V       |
| $V_{OL2}$ | Output Low Voltage | $V_{CC} < 2.5$ V, $I_{OL} = 1.0$ mA    |                     | 0.2           | V       |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 5. PIN IMPEDANCE CHARACTERISTICS**

| Symbol            | Parameter                      | Conditions     | Max | Unit |
|-------------------|--------------------------------|----------------|-----|------|
| $C_{IN}$ (Note 5) | SDA I/O Pin Capacitance        | $V_{IN} = 0$ V | 8   | pF   |
| $C_{IN}$ (Note 5) | Input Capacitance (other pins) | $V_{IN} = 0$ V | 6   | pF   |

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.



Table 6. A.C. CHARACTERISTICS (Note 6)

| Symbol                   | Parameter                                  | Standard<br>$V_{CC} = 1.7\text{ V} - 5.5\text{ V}$ |       | Fast<br>$V_{CC} = 1.7\text{ V} - 5.5\text{ V}$ |      | Fast-Plus<br>$V_{CC} = 1.7\text{ V} - 5.5\text{ V}$ |       | Unit          |
|--------------------------|--------------------------------------------|----------------------------------------------------|-------|------------------------------------------------|------|-----------------------------------------------------|-------|---------------|
|                          |                                            | Min                                                | Max   | Min                                            | Max  | Min                                                 | Max   |               |
| $F_{SCL}$                | Clock Frequency                            |                                                    | 100   |                                                | 400  |                                                     | 1,000 | kHz           |
| $t_{HD:STA}$             | START Condition Hold Time                  | 4                                                  |       | 0.6                                            |      | 0.25                                                |       | $\mu\text{s}$ |
| $t_{LOW}$                | Low Period of SCL Clock                    | 4.7                                                |       | 1.3                                            |      | 0.45                                                |       | $\mu\text{s}$ |
| $t_{HIGH}$               | High Period of SCL Clock                   | 4                                                  |       | 0.6                                            |      | 0.40                                                |       | $\mu\text{s}$ |
| $t_{SU:STA}$             | START Condition Setup Time                 | 4.7                                                |       | 0.6                                            |      | 0.25                                                |       | $\mu\text{s}$ |
| $t_{HD:DAT}$             | Data In Hold Time                          | 0                                                  |       | 0                                              |      | 0                                                   |       | $\mu\text{s}$ |
| $t_{SU:DAT}$             | Data In Setup Time                         | 250                                                |       | 100                                            |      | 50                                                  |       | ns            |
| $t_R$ (Note 7)           | SDA and SCL Rise Time                      |                                                    | 1,000 | 20                                             | 300  |                                                     | 100   | ns            |
| $t_F$ (Note 7)           | SDA and SCL Fall Time                      |                                                    | 300   | 20                                             | 300  |                                                     | 100   | ns            |
| $t_{SU:STO}$             | STOP Condition Setup Time                  | 4                                                  |       | 0.6                                            |      | 0.25                                                |       | $\mu\text{s}$ |
| $t_{BUF}$                | Bus Free Time Between STOP and START       | 4.7                                                |       | 1.3                                            |      | 0.5                                                 |       | $\mu\text{s}$ |
| $t_{AA}$                 | SCL Low to Data Out Valid                  |                                                    | 3.5   |                                                | 0.9  |                                                     | 0.40  | $\mu\text{s}$ |
| $t_{DH}$                 | Data Out Hold Time                         | 100                                                |       | 100                                            |      | 50                                                  |       | ns            |
| $T_i$ (Note 7)           | Noise Pulse Filtered at SCL and SDA Inputs |                                                    | 100   |                                                | 50   |                                                     | 50    | ns            |
| $t_{WR}$                 | Write Cycle Time                           |                                                    | 5     |                                                | 5    |                                                     | 5     | ms            |
| $t_{PU}$<br>(Notes 7, 8) | Power-up to Ready Mode                     |                                                    | 0.35  |                                                | 0.35 |                                                     | 0.35  | ms            |

6. Test conditions according to "A.C. Test Conditions" table.

7. Tested initially and after a design or process change that affects this parameter.

8.  $t_{PU}$  is the delay between the time  $V_{CC}$  is stable and the device is ready to accept commands.

Table 7. A.C. TEST CONDITIONS

|                           |                                                                                                                                                  |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Input Levels              | $0.2 \times V_{CC}$ to $0.8 \times V_{CC}$                                                                                                       |
| Input Rise and Fall Times | $\leq 50\text{ ns}$                                                                                                                              |
| Input Reference Levels    | $0.3 \times V_{CC}$ , $0.7 \times V_{CC}$                                                                                                        |
| Output Reference Levels   | $0.5 \times V_{CC}$                                                                                                                              |
| Output Load               | Current Source; $I_{OL} = 3\text{ mA}$ ( $V_{CC} \geq 2.5\text{ V}$ ); $I_{OL} = 1\text{ mA}$ ( $V_{CC} < 2.5\text{ V}$ ); $C_L = 100\text{ pF}$ |

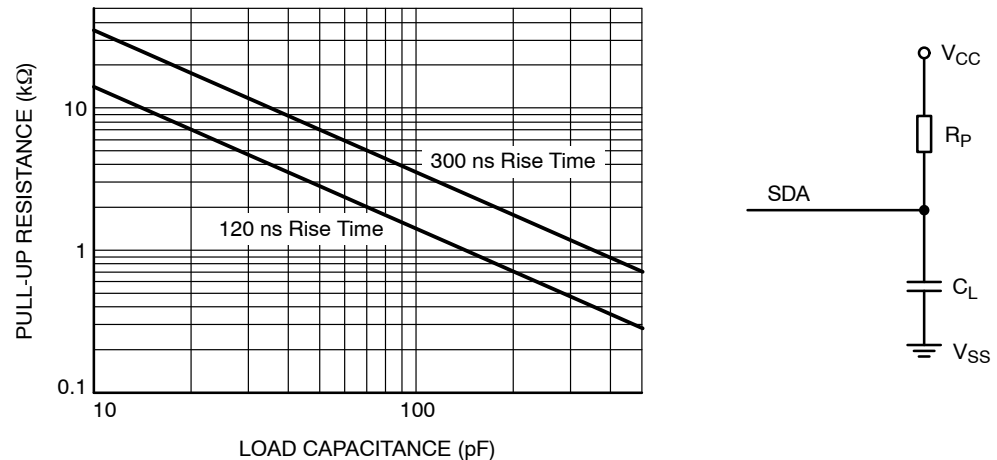


Figure 2. Maximum Pull-up Resistance vs. Load Capacitance

## POWER-ON RESET (POR)

The CAT24S128 incorporates Power-On Reset (POR) circuitry which protects the device against powering up in the wrong state.

The CAT24S128 will power up into Standby mode after  $V_{CC}$  exceeds the POR trigger level and will power down into Reset mode when  $V_{CC}$  drops below the POR trigger level. This bi-directional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

## PIN DESCRIPTION

**SCL:** The Serial Clock input pin accepts the Serial Clock generated by the Master.

**SDA:** The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

## FUNCTIONAL DESCRIPTION

The CAT24S128 supports the Inter-Integrated Circuit ( $I^2C$ ) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24S128 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs  $A_0$ ,  $A_1$ , and  $A_2$ .

## $I^2C$ BUS PROTOCOL

The  $I^2C$  bus consists of two 'wires', SCL and SDA. The two wires are connected to the  $V_{CC}$  supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting

device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 3). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

## Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 4). The next 3 bits are set to 0 0 1. The last bit,  $R/\overline{W}$ , specifies whether a Read (1) or Write (0) operation is to be performed.

## Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9<sup>th</sup> clock cycle (Figure 5). The Slave will also acknowledge all address bytes and every data byte presented in Write mode if the addressed location is not write protected. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9<sup>th</sup> clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 6.

CAT24S128

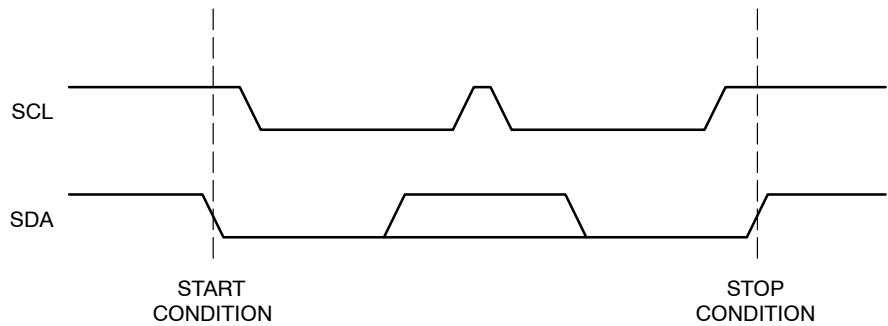


Figure 3. START/STOP Conditions

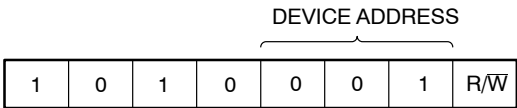


Figure 4. Slave Address Bits

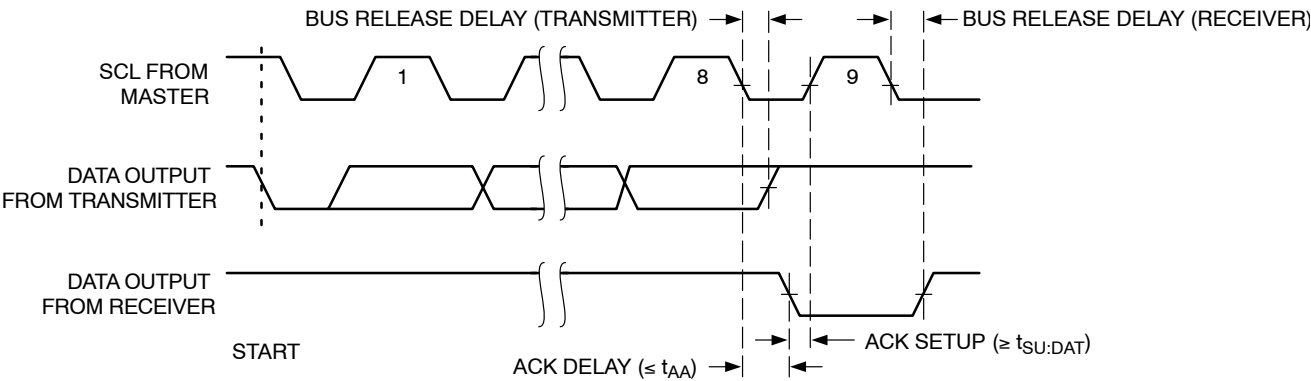


Figure 5. Acknowledge Timing

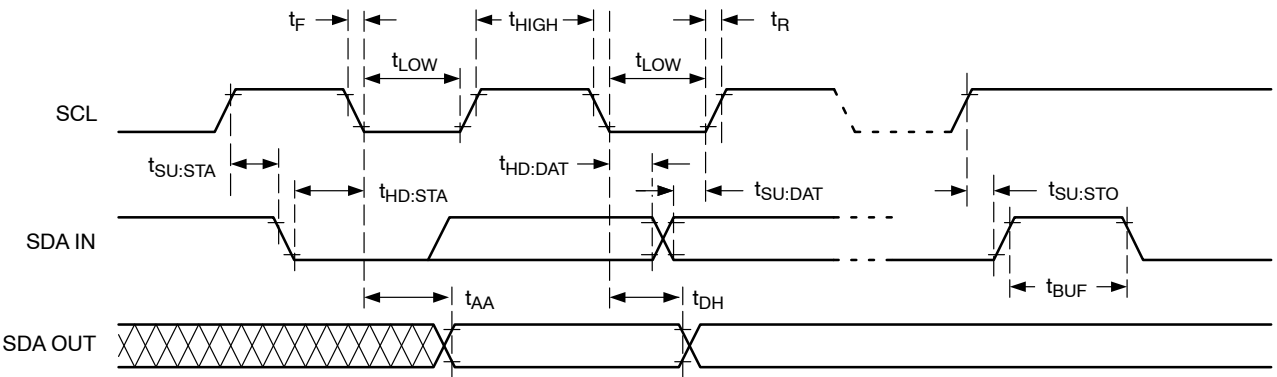


Figure 6. Bus Timing

## WRITE OPERATIONS

### Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address (Table 8) and data to be written (Figure 7). The Slave, CAT24S128 acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 8). During the internal Write cycle ( $t_{WR}$ ), the CAT24S128 will not acknowledge any Read or Write request from the Master.

### Page Write

The CAT24S128 contains 16,384 bytes of data, arranged in 256 pages of 64 bytes each. A two byte address word (Table 8), following the Slave address, points to the first byte to be written into the memory array. The most significant 8 bits from the address active bits (a13 to a6) identify the page and the last 6 bits (a5 to a0) identify the byte within the page. Up to 64 bytes can be written in one Write cycle (Figure 9). The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 64 data bytes, then earlier bytes will be overwritten by later bytes in a ‘wrap-around’ fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

### Acknowledge Polling

The ready/busy status of the CAT24S128 can be ascertained by sending Read or Write requests immediately following the STOP condition that initiated the internal Write cycle. As long as internal Write is in progress, the CAT24S128 will not acknowledge the Slave address.

### Software Write Protection

The user can select to write-protect partial or full memory array by writing a specific data into the Write Protect Register (WPR). The WPR is located outside of the 16K bytes memory addressing space, at address 1xxx xxxx xxxx xxxx.

The software write protect control bits from the Write Protect Register are shown in Table 9. The write protect control bits, b0 to b3 are non-volatile.

The WPEN (Write Protect Enable) bit enables the write protection when it is set to “1”. When the WPEN bit is “0”, the whole memory array can be written.

The BP0 and BP1 (Block Protect) bits determine which area is write protected. The user can select to protect a quarter, one half, three quarters or the entire memory by setting these bits according to Table 10. The protected blocks then become read-only.

The least significant bit from the Write Protect Register, WPL allows the user to lock the write protection status. When the WPL bit is set to “1” the control bits, b0 to b3 from WPR cannot be modified. Therefore the protected blocks can be permanently protected. If WPL bit is “0” the status of control bits from the WPR can be changed.

The CAT24S128 will not acknowledge the data byte and the write request will be rejected for the addresses located in the protected area.

NOTE: Once the WPL bit is set to “1”, the user can no longer modify the WPR bits, therefore the write protection status is permanently locked.

**Table 8. BYTE ADDRESS**

|                        | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|------------------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| Memory Array           | 0   | x   | a13 | a12 | a11 | a10 | a9 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| Write Protect Register | 1   | x   | x   | x   | x   | x   | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  |

**Table 9. WRITE PROTECT REGISTER**

| b7 | b6 | b5 | b4 | b3   | b2  | b1  | b0  |
|----|----|----|----|------|-----|-----|-----|
| 0  | 0  | 0  | 0  | WPEN | BP1 | BP0 | WPL |

**Table 10. BLOCK PROTECTION**

| BP1 | BP0 | Array Address Protected | Protection                 |
|-----|-----|-------------------------|----------------------------|
| 0   | 0   | 3000 - 3FFF             | Upper Quarter Protection   |
| 0   | 1   | 2000 - 3FFF             | Upper Half Protection      |
| 1   | 0   | 1000 - 3FFF             | Upper 3/4 Array Protection |
| 1   | 1   | 0000 - 3FFF             | Full Array Protection      |

## Writing the Write Protect Register

The write operation to the Write Protect Register is performed using a Byte Write instruction (Figure 7) at address 1xxx xxxx xxxx xxxx. The data byte contains the 4

least significant bits as significant bits. The b7 to b4 bits are don't care during the write operation. Sending more than one data byte will cancel the write cycle (Write Protect Register content will not be changed).

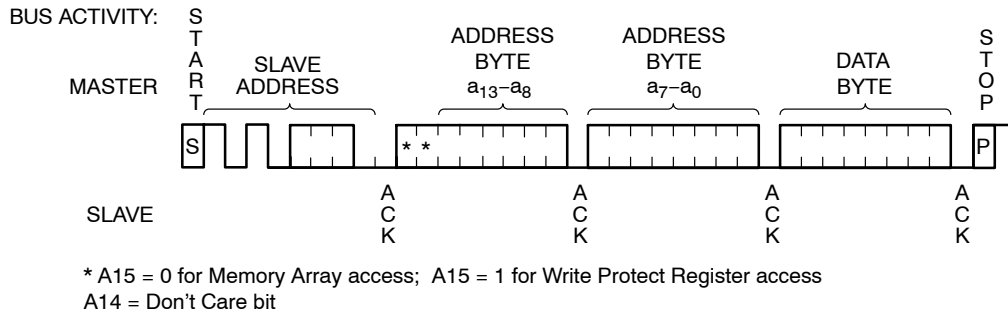


Figure 7. Byte Write Sequence

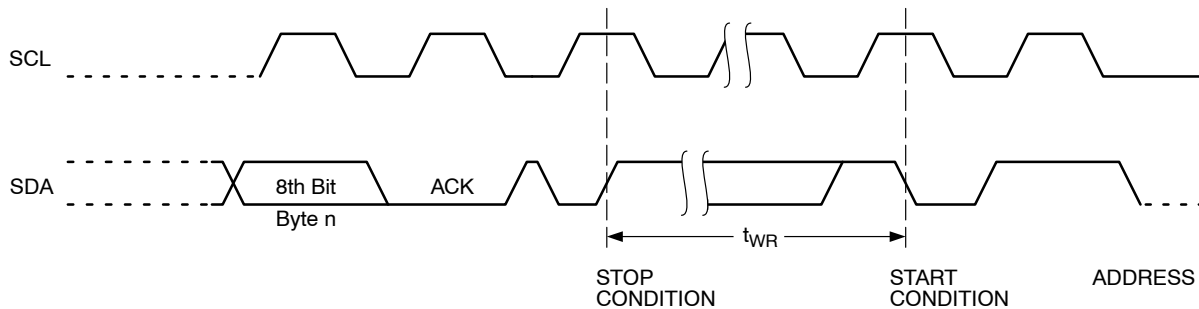


Figure 8. Write Cycle Timing

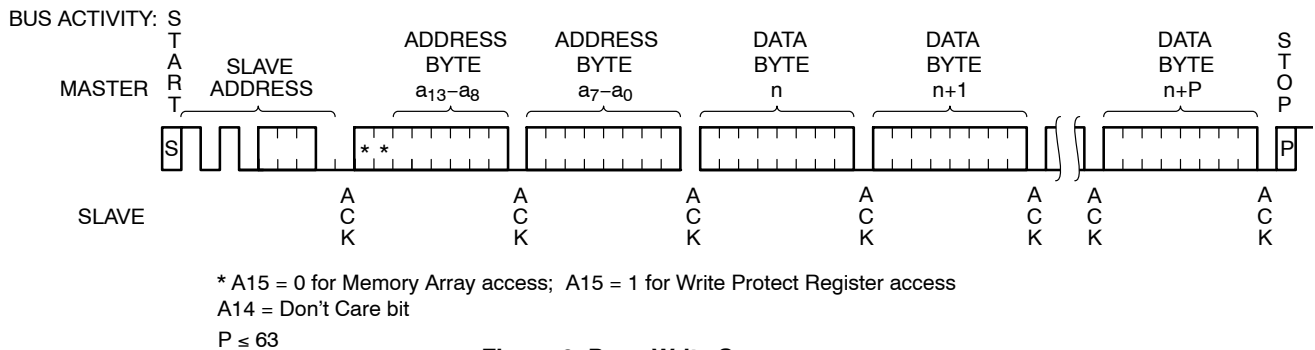


Figure 9. Page Write Sequence

## READ OPERATIONS

### Immediate Read

Upon receiving a Slave address with the  $R/\overline{W}$  bit set to '1', the CAT24S128 will interpret this as a request for data residing at the current byte address in memory. The CAT24S128 will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAT24S128 returns to Standby mode.

### Selective Read

To read data residing at a specific location, the internal address counter must first be initialized as described under Byte Write. If rather than following up the two address bytes with data, the Master instead follows up with an Immediate Read sequence, then the CAT24S128 will use the 14 active address bits to initialize the internal address counter and will shift out data residing at the corresponding location. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 11), the CAT24S128 returns to Standby mode.

### Sequential Read

If during a Read session the Master acknowledges the 1<sup>st</sup> data byte, then the CAT24S128 will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).

### Write Protect Register Read

To read the Write Protect Register, the master simply sends a Selective Read instruction (Figure 12) at address 1xxx xxxx xxxx xxxx. The data byte shifted out by the device shows the content of the WPR according to Table 9. If the master acknowledges the data byte and send more clocks, the WPR content will continue to be read out.

### Delivery State

The CAT24S128 is shipped erased, i.e., all memory array bytes are FFh and the Write Protect Register bits set to 0 (00h).

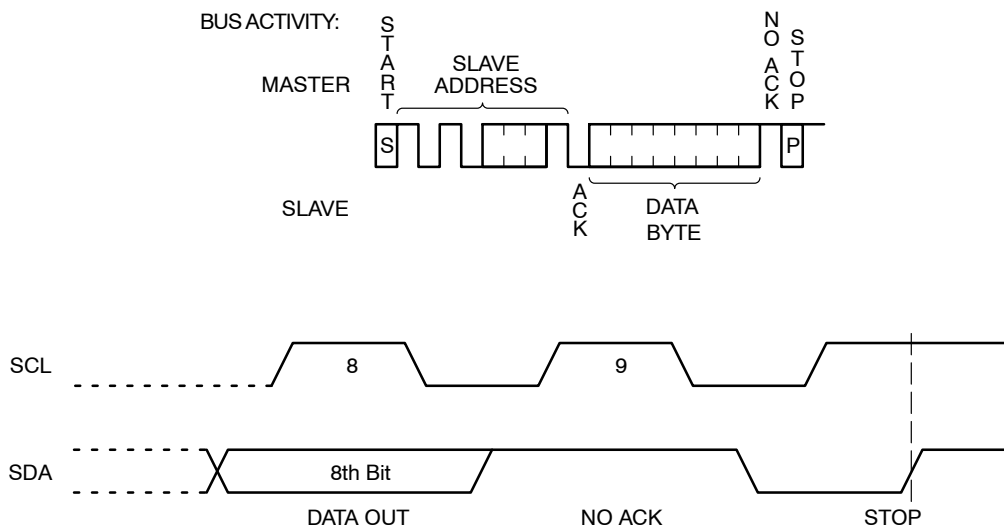


Figure 10. Immediate Read Sequence and Timing

## CAT24S128

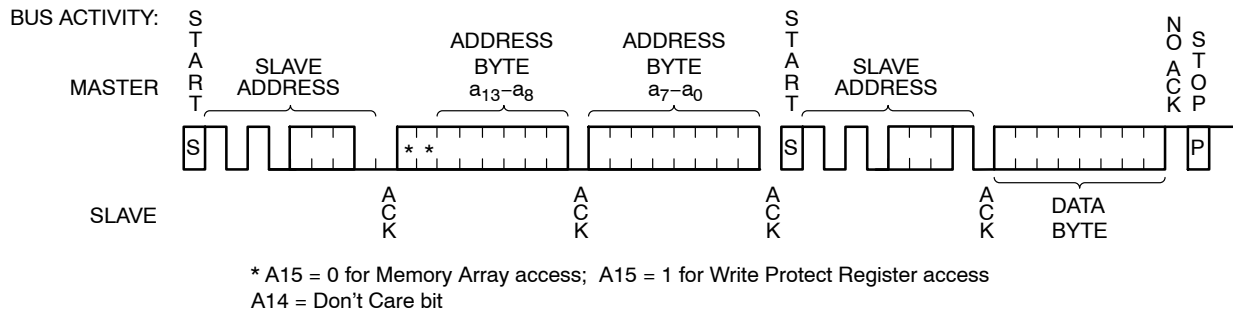


Figure 11. Selective Read Sequence

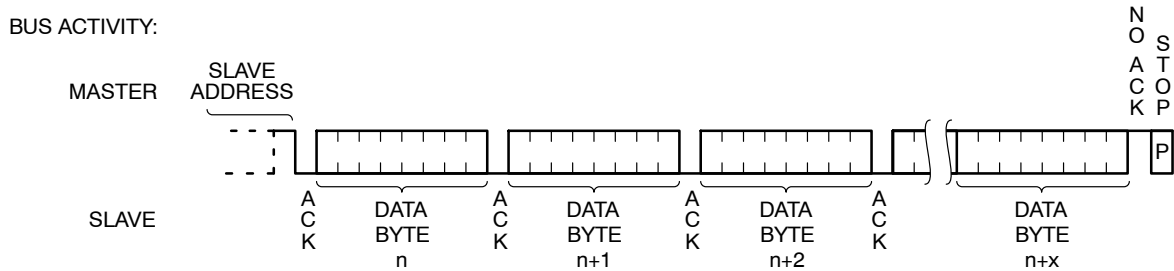


Figure 12. Sequential Read Sequence

### ORDERING INFORMATION (Notes 9 thru 11)

| Device Order Number | Specific Device Marking | Package Type | Temperature Range                | Lead Finish | Shipping <sup>†</sup> |
|---------------------|-------------------------|--------------|----------------------------------|-------------|-----------------------|
| CAT24S128C4ATR      | E                       | WLCSP 4-ball | Industrial<br>(-40 °C to +85 °C) | N/A         | 5,000 / Tape & Reel   |
| CAT24S128C4UTR      | E                       | WLCSP 4-ball | Industrial<br>(-40 °C to +85 °C) | N/A         | 5,000 / Tape & Reel   |

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

9. All packages are RoHS-compliant (Pb-Free, Halogen-free).

10. For detailed information and a breakdown of device nomenclature and numbering systems, please see the **onsemi** Device Nomenclature document, [TND310/D](#), available at [www.onsemi.com](#)

11. **Caution: The EEPROM devices delivered in WLCSP must never be exposed to ultraviolet light. When exposed to ultraviolet light the EEPROM cells lose their stored data.**

## CAT24S128

### REVISION HISTORY

| Revision | Description of Changes                            | Date       |
|----------|---------------------------------------------------|------------|
| 9        | Rebranded the Data Sheet to <b>onsemi</b> format. | 09/03/2025 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



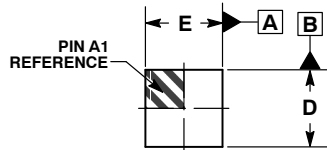




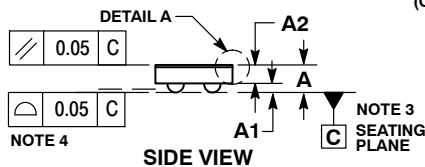
SCALE 4:1

**WLCSP4, 0.84x0.84**  
CASE 567PC  
ISSUE A

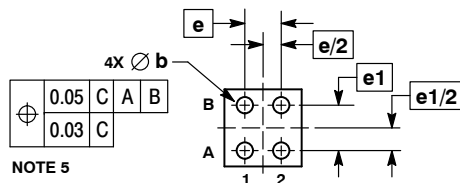
DATE 30 MAY 2017



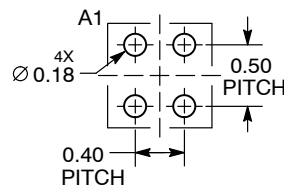
TOP VIEW



SIDE VIEW



BOTTOM VIEW

**RECOMMENDED  
SOLDERING FOOTPRINT\***


DIMENSIONS: MILLIMETERS

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.
6. BACKSIDE COATING IS OPTIONAL.

| MILLIMETERS |      |           |      |
|-------------|------|-----------|------|
| DIM         | MIN  | NOM       | MAX  |
| A           |      |           | 0.30 |
| A1          | 0.08 | 0.10      | 0.12 |
| A2          |      | 0.15 REF  |      |
| A3          |      | 0.025 REF |      |
| b           | 0.16 | 0.18      | 0.20 |
| D           | 0.81 | 0.84      | 0.87 |
| E           | 0.81 | 0.84      | 0.87 |
| e           |      | 0.40 BSC  |      |
| e1          |      | 0.50 BSC  |      |

**GENERIC  
MARKING DIAGRAM\***


- X = Specific Device Code  
Y = Year  
W = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                          |                                                                                                                                                                                  |
|-------------------------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| <b>DESCRIPTION:</b>     | <b>WLCSP4, 0.84X0.84</b> | <b>PAGE 1 OF 1</b>                                                                                                                                                               |

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