AMIS−30663

High Speed CAN Transceiver

ON Semiconductor®

http://onsemi.com

Introduction

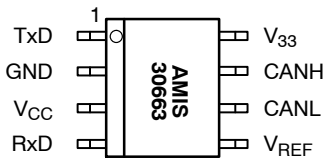
The AMIS−30663 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The digital interface level is powered from a 3.3 V supply providing true I/O voltage levels for 3.3 V CAN controllers.

The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller. Due to the wide common−mode voltage range of the receiver inputs, the AMIS−30663 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

Key Features

- Fully Compatible with the “ISO 11898−2” Standard
- Certified “Authentication on CAN Transceiver Conformance (d1.1)”
- High Speed (up to 1 Mbit/s)
- Ideally Suited for 12 V and 24 V Industrial and Automotive Applications
- Low EME Common−mode−choke is No Longer Required
- Differential Receiver with Wide Common−mode Range (±35 V) for High EMS
- No Disturbance of the Bus Lines with an Un−powered Node
- Transmit Data (TxD) Dominant Time−out Function
- Thermal Protection
- Bus Pins Protected Against Transients in an Automotive Environment
- Short Circuit Proof to Supply Voltage and Ground
- Logic Level Inputs Compatible with 3.3 V Devices
- ESD Protection Level for CAN Bus up to ±8 kV
- This is a Pb−Free Device

PIN ASSIGNMENT



(Top View)

Table 1. Ordering Information

Part Number	Description	Package	Container		Temp. Range
			Shipping Configuration†	Quantity	
AMIS30663CANG2G	HS CAN Transc. (3.3 V)	SOIC−8 GREEN	Tube/Tray	96	−40°C to 125°C
AMIS30663CANG2RG	HS CAN Transc. (3.3 V)	SOIC−8 GREEN	Tape & Reel	3000	−40°C to 125°C

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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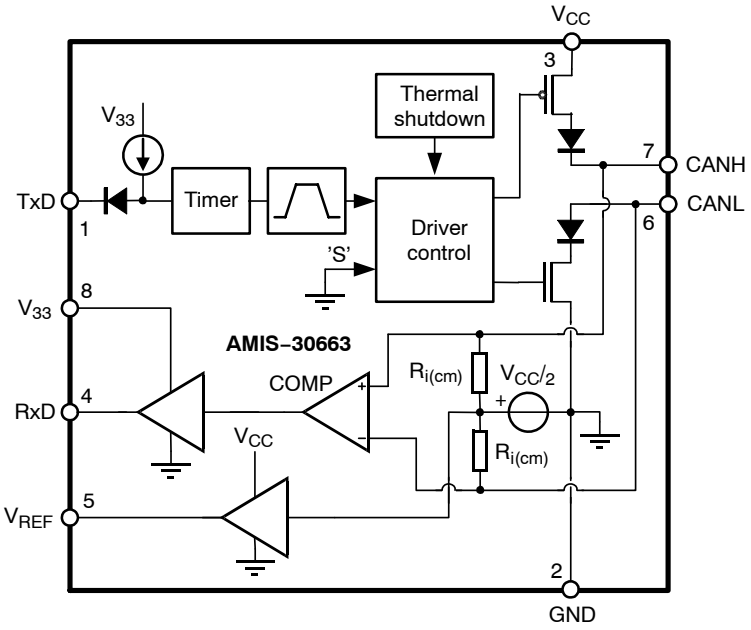


Figure 1. Block Diagram

Table 2. Technical Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CANH}	DC voltage at pin CANH	0 < VCC < 5.25 V; no time limit	−45	+45	V
V_{CANL}	DC voltage at pin CANL	0 < VCC < 5.25 V; no time limit	−45	+45	V
Vo(dif)(bus_dom)	Differential bus output voltage in dominant state	42.5 Ω < RLT < 60 Ω	1.5	3	V
tpd(rec−dom)	Propagation delay TxD to RxD	Figure 7	100	230	ns
$t_{pd(dom-rec)}$	Propagation delay TxD to RxD	Figure 7	100	245	ns
CM−range	Input common−mode range for comparator	Guaranteed differential receiver threshold and leakage current	−35	+35	V
$V_{CM-peak}$	Common−mode peak	Figures 8 and 9 (Note 1)	−500	500	mV
$V_{CM-step}$	Common−mode step	Figures 8 and 9 (Note 1)	−150	150	mV

1. The parameters VCM−peak and VCM−step guarantee low EME.

Typical Application

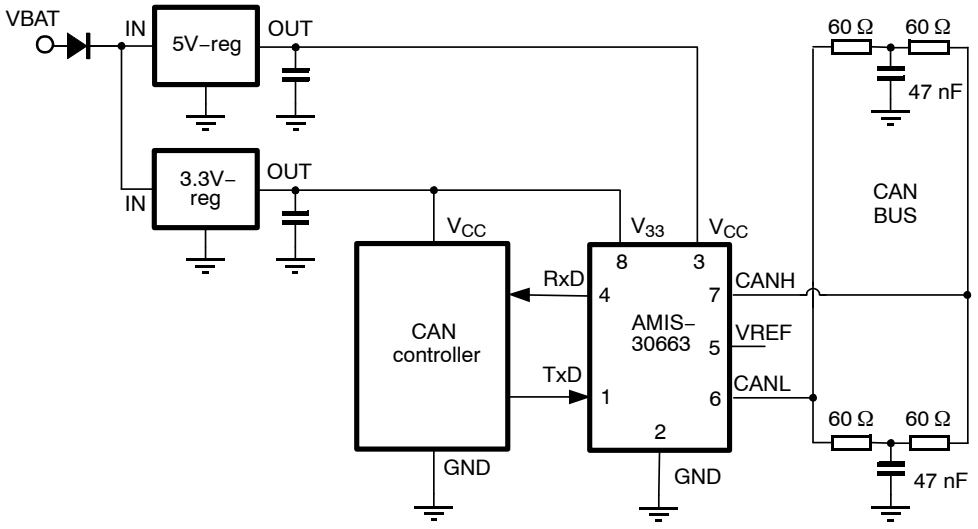
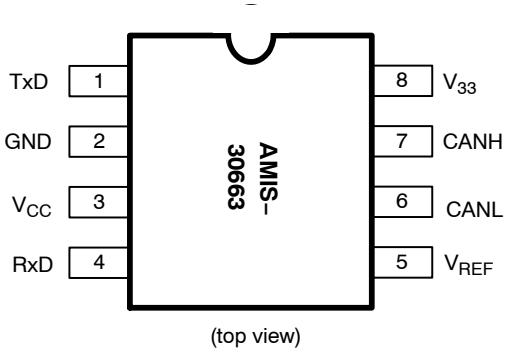


Figure 2. Application Diagram



(top view)

Figure 3. Pin Configuration

Table 3. Pin Out

Pin	Name	Description
1	TxD	Transmit data input; low input → dominant driver; internal pull−up current
2	GND	Ground
3	V_{CC}	Supply voltage
4	RxD	Receive data output; dominant transmitter → low output
5	V_{REF}	Reference voltage output
6	CANL	LOW−level CAN bus line (low in dominant mode)
7	CANH	HIGH−level CAN bus line (high in dominant mode)
8	V_{33}	3.3 V supply for digital I/O

Functional Description

General

The AMIS−30663 is the interface between the CAN protocol controller and the physical bus. It is intended for use in automotive and industrial applications requiring baud rates up to 1 Mbaud. It provides differential transmit capability to the bus and differential receiver capability to the CAN protocol controller. It is fully compatible to the "ISO 11898−2" standard.

Operating Modes

AMIS−30663 only operates in high−speed mode as illustrated in Table 4.

The transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimised to give extremely low EME.

Table 4. Function Table (X = don't care)

Mode	Pin		Bus		
	TxD	RxD	State	CANH	CANL
4.75 V < Vcc < 5.25 V					
High Speed	0	0	Dominant	High	Low
	1	1	Recessive	0.5 Vcc	0.5 Vcc
Vcc < PORL					
−	X	1	Recessive	$0 < V_{CANH} < V_{CC}$	$0 < V_{CANL} < V_{CC}$
PORL < Vcc < 4.75 V					
−	$> V_{IH}$	1	Recessive	$0 < V_{CANH} < V_{CC}$	$0 < V_{CANL} < V_{CC}$

Over−temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when pin TxD goes HIGH. The thermal protection circuit is particularly needed when a bus line short circuits.

TxD Dominant Time−out Function

A TxD dominant time−out timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the LOW−level on pin TxD exceeds the internal timer value t_{dom}, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

Fail−safe Features

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short−circuit to either positive or negative supply voltage − although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to "ISO 7637"; see Figure 4).

Should TxD become disconnected, this pin is pulled high internally.

When the Vcc supply is removed, pins TxD and RxD will be floating. This prevents the AMIS−30663 from being supplied by the CAN controller through the I/O pins.

3.3 V Interface

AMIS−30663 may be used to interface with 3.3 V or 5 V controllers by use of the V_{33} pin. This pin may be supplied with 3.3 V or 5 V to have the corresponding digital interface voltage levels.

When the V_{33} pin is supplied at 2.5 V, even interfacing with 2.5 V CAN controllers is possible. See also Digital Output Characteristics @ V_{33} = 2.5 V, Table 8. In this case a pull resistor from TxD to V_{33} is necessary.

Electrical Characteristics

Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means that the current is flowing into the pin. Sourcing current means that the current is flowing out of the pin.

Absolute Maximum Ratings

Stresses above those listed in Table 5 may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may effect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage		−0.3	+7	V
V_{33}	I/O interface voltage		−0.3	+7	V
V_{CANH}	DC voltage at pin CANH	0 < V_{CC} < 5.25 V; no time limit	−45	+45	V
V_{CANL}	DC voltage at pin CANL	0 < V_{CC} < 5.25 V; no time limit	−45	+45	V
V_{TxD}	DC voltage at pin TxD		−0.3	V_{CC} + 0.3	V
V_{RxD}	DC voltage at pin RxD		−0.3	V_{CC} + 0.3	V
VREF	DC voltage at pin VREF		−0.3	VCC + 0.3	V
$V_{tran(CANH)}$	Transient voltage at pin CANH	(Note 2)	−150	+150	V
$V_{tran(CANL)}$	Transient voltage at pin CANL	(Note 2)	−150	+150	V
$V_{tran(VREF)}$	Transient voltage at pin VREF	(Note 2)	−150	+150	V
$V_{esd(CANL/CANH)}$	Electrostatic discharge voltage at CANH and CANL pin	(Note 3) (Note 6)	−8 −500	+8 +500	kV V
V_{esd}	Electrostatic discharge voltage at all other pins	(Note 4) (Note 6)	−4 −250	+ 4 +250	kV V
Latch−up	Static latch−up at all pins	(Note 5)		100	mA
T_{stg}	Storage temperature		−55	+155	°C
T_{amb}	Ambient temperature		−40	+125	°C
T_{junc}	Maximum junction temperature		−40	+150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Applied transient waveforms in accordance with “ISO 7637 part 3”, test pulses 1, 2, 3a and 3b (see Figure 4).
3. Standardized human body model system ESD pulses in accordance to IEC 1000.4.2.
4. Standardized human body model ESD pulses in accordance to MIL883 method 3015. Supply pin 8 is ±4 kV.
5. Static latch−up immunity: static latch−up protection level when tested according to EIA/JESD78.
6. Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3−1993.

Table 6. Thermal Characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj-a)}$	Thermal resistance from junction to ambient in SO8 package	In free air	145	K/W
$R_{th(vj-s)}$	Thermal resistance from junction to substrate of bare die	In free air	45	K/W

Table 7. DC Characteristics

(V_{CC} = 4.75 to 5.25 V; V_{33} = 2.9 V to 3.6 V; T_{junc} = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply (pin V_{CC} and pin V_{33})						
I_{CC}	Supply current	Dominant; V_{TXD} = 0 V Recessive; V_{TXD} = V_{CC}		45 4	65 8	mA
I_{33}	I/O interface current	V_{33} = 3.3 V; C_L = 20 pF; recessive			1	μA
I_{33}	I/O interface current (Note 7)	V_{33} = 3.3 V; C_L = 20 pF; 1 Mbps			170	μA
Transmitter Data Input (pin TxD)						
V_{IH}	HIGH−level input voltage	Output recessive	2.0	−	V_{CC}	V
V_{IL}	LOW−level input voltage	Output dominant	−0.3	−	+0.8	V
I_{IH}	HIGH−level input current	V_{TxD} = V_{33}	−1	0	+1	μA
I_{IL}	LOW−level input current	V_{TxD} = 0 V	−50	−200	−300	μA

7. Not tested on ATE.

Table 7. DC Characteristics

(V_{CC} = 4.75 to 5.25 V; V_{33} = 2.9 V to 3.6 V; T_{junc} = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Transmitter Data Input (pin TxD)						
C_i	Input capacitance (Note 7)		−	5	10	pF
Receiver Data Output (pin RxD)						
V_{OH}	HIGH−level output voltage	I_{RXD} = − 10 mA	0.7 x V_{33}	0.75 x V_{33}		V
V_{OL}	LOW−level output voltage	I_{RXD} = 5 mA		0.18	0.35	V
I_{oh}	HIGH−level output current (Note 7)	V_{RxD} = 0.7 x V_{33}	−10	−15	−20	mA
I_{ol}	LOW−level output current (Note 7)	V_{RxD} = 0.45 V	5	10	15	mA
Reference Voltage Output (pin V_{REF})						
V_{REF}	Reference output voltage	−50 μA < I_{VREF} < +50 μA	0.45 x V_{CC}	0.50 x V_{CC}	0.55 x V_{CC}	V
V_{REF_CM}	Reference output voltage for full common−mode range	−35 V < V_{CANH} < +35 V; −35 V < V_{CANL} < +35 V	0.40 x V_{CC}	0.50 x V_{CC}	0.60 x V_{CC}	V
Bus Lines (pins CANH and CANL)						
$V_{o(reces)(CANH)}$	Recessive bus voltage at pin CANH	V_{TxD} = V_{CC}; no load	2.0	2.5	3.0	V
$V_{o(reces)(CANL)}$	Recessive bus voltage at pin CANL	V_{TxD} = V_{CC}; no load	2.0	2.5	3.0	V
$I_{o(reces)\ (CANH)}$	Recessive output current at pin CANH	−35 V < V_{CANH} < +35 V; 0 V < V_{CC} < 5.25 V	−2.5	−	+2.5	mA
$I_{o(reces)\ (CANL)}$	Recessive output current at pin CANL	−35 V < V_{CANL} < +35 V; 0 V < V_{CC} < 5.25 V	−2.5	−	+2.5	mA
$V_{o(dom)\ (CANH)}$	Dominant output voltage at pin CANH	V_{TxD} = 0 V	3.0	3.6	4.25	V
$V_{o(dom)\ (CANL)}$	Dominant output voltage at pin CANL	V_{TxD} = 0 V	0. 5	1.4	1.75	V
$V_{o(dif)\ (bus)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = 0 V; dominant; 42.5 Ω < R_{LT} < 60 Ω	1.5	2.25	3.0	V
		V_{TxD} = V_{CC}; recessive; no load	−120	0	+50	mV
$I_{o(sc)\ (CANH)}$	Short circuit output current at pin CANH	V_{CANH} = 0 V; V_{TxD} = 0 V	−45	−70	−95	mA
$I_{o(sc)\ (CANL)}$	Short circuit output current at pin CANL	V_{CANL} = 36 V; V_{TxD} = 0 V	45	70	120	mA
$V_{i(dif)(th)}$	Differential receiver threshold voltage	−5 V < V_{CANL} < +12 V; −5 V < V_{CANH} < +12 V; see Figure 5	0.5	0.7	0.9	V
$V_{ihcm(dif)\ (th)}$	Differential receiver threshold voltage for high common−mode	−35 V < V_{CANL} < +35 V; −35 V < V_{CANH} < +35 V; see Figure 5	0.25	0.7	1.05	V
$V_{i(dif)\ (hys)}$	Differential receiver input voltage hysteresis	−35 V < V_{CANL} < +35 V; −35 V < V_{CANH} < +35 V; see Figure 5	50	70	100	mV
Bus Lines (pins CANH and CANL)						
$R_{i(cm)(CANH)}$	Common−mode input resistance at pin CANH		15	25	37	KΩ
$R_{i(cm)\ (CANL)}$	Common−mode input resistance at pin CANL		15	25	37	KΩ
$R_{i(cm)(m)}$	Matching between pin CANH and pin CANL common−mode input resistance	V_{CANH} = V_{CANL}	−3	0	+3	%

7. Not tested on ATE.

Table 7. DC Characteristics

(V_{CC} = 4.75 to 5.25 V; V_{33} = 2.9 V to 3.6 V; T_{junc} = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Bus Lines (pins CANH and CANL)						
$R_{i(dif)}$	Differential input resistance		25	50	75	KΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	V_{TxD} = V_{CC}; not tested		7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	V_{TxD} = V_{CC}; not tested		7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	V_{TxD} = V_{CC}; not tested		3.75	10	pF
$I_{LI(CANH)}$	Input leakage current at pin CANH	V_{CC} = 0 V; V_{CANH} = 5 V	10	170	250	μA
$I_{LI(CANL)}$	Input leakage current at pin CANL	V_{CC} = 0 V; V_{CANL} = 5 V	10	170	250	μA
$V_{CM-peak}$	Common−mode peak during transition from dom → rec or rec → dom	Figures 8 and 9	−500		500	mV
$V_{CM-step}$	Difference in common−mode between dominant and recessive state	Figures 8 and 9	−150		150	mV
Power on Reset						
PORL	POR level	CANH, CANL, V_{ref} in tri−state below POR level	2.2	3.5	4.7	V
Thermal Shutdown						
$T_{j(sd)}$	shutdown junction temperature		150	160	180	°C
Timing Characteristics (see Figures 6 and 7)						
$t_{d(TxD-BUSon)}$	Delay TxD to bus active		40	85	110	ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive		30	60	110	ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxD		25	55	110	ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD		65	100	135	ns
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD from recessive to dominant		100		230	ns
$t_{d(dom-rec)}$	Propagation delay TxD to RxD from dominant to recessive		100		245	ns
$t_{dom(TxD)}$	TxD dominant time for time out	V_{TxD} = 0 V	250	450	750	μs

7. Not tested on ATE.

Table 8. Digital Output Characteristics @ V_{33} = 2.5 V

(V_{CC} = 4.75 to 5.25 V; V_{33} = 2.5 V ±5%; T_{junc} = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Receiver Data Output (pin RxD)						
I_{oh}	HIGH−level output current	V_{OH} > 0.9 x V_{33}	−2.6			mA
I_{ol}	LOW−level output current	V_{OL} < 0.1 x V_{33}			4	mA

Measurement Set−ups and Definitions

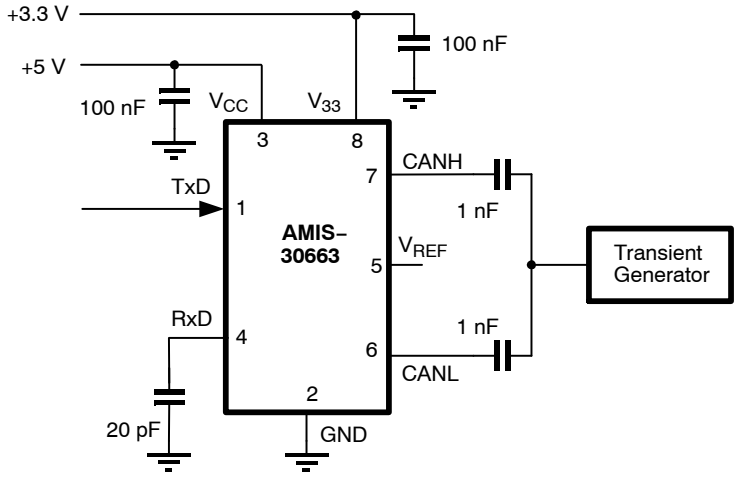


Figure 4. Test Circuit for Automotive Transients

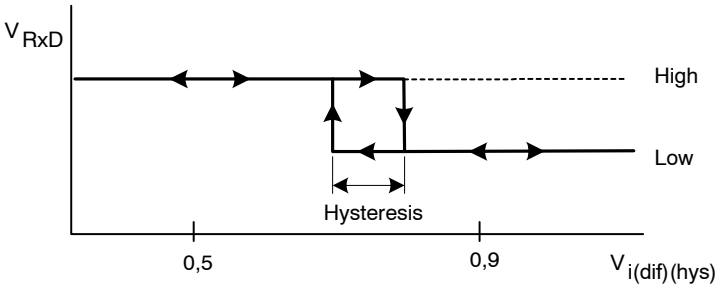


Figure 5. Hysteresis of the Receiver

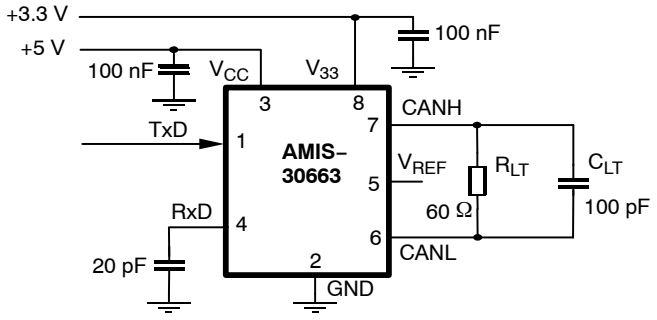


Figure 6. Test Circuit for Timing Characteristics

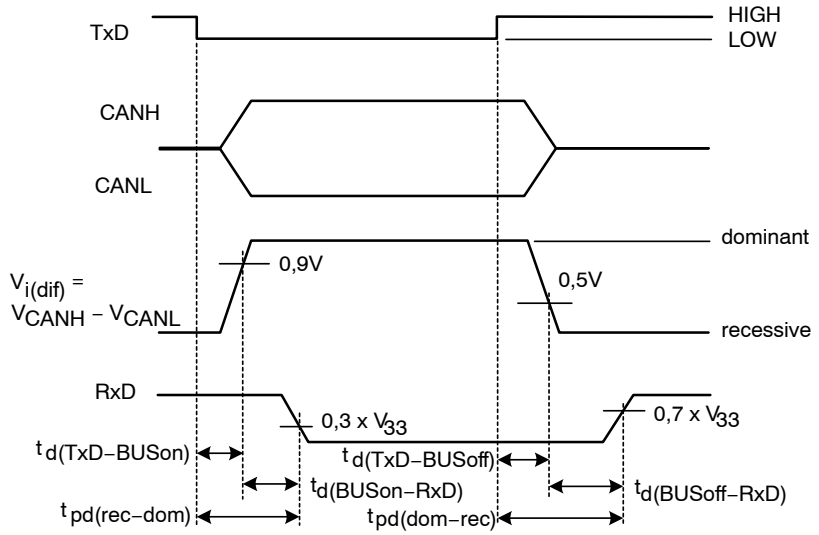


Figure 7. Timing Diagram for AC Characteristics

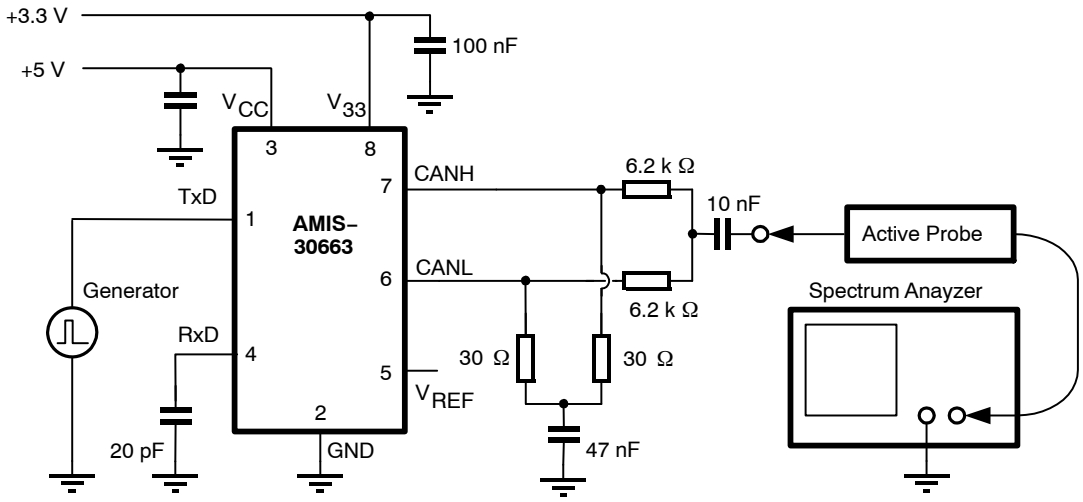


Figure 8. Basic Test Set−up for Electromagnetic Measurement

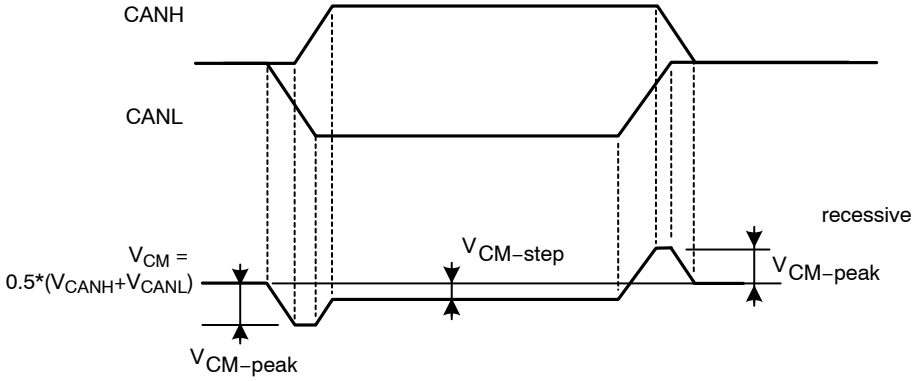


Figure 9. Common−mode Voltage Peaks (see measurement set−up Figure 8)

Soldering

Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in−depth account of soldering ICs can be found in the ON Semiconductor “Data Handbook IC26; Integrated Circuit Packages” (document order number 9398 652 90011). There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed−circuit boards (PCB) with high population densities. In these situations re−flow soldering is often used.

Re−flow Soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the PCB by screen printing, stencilling or pressure−syringe dispensing before package placement. Several methods exist for re−flowing; for example, infrared/convection heating in a conveyor type oven.

Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method. Typical re−flow peak temperatures range from 215 to 250°C. The top−surface temperature of the packages should preferably be kept below 230°C.

Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or PCBs with a high component density, as solder bridging and non−wetting can present major problems. To overcome these problems the double−wave soldering method was specifically developed. If wave soldering is used the following conditions must be observed for optimal results:

- Use a double−wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  1. Larger than or equal to 1.27 mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the PCB;
  2. Smaller than 1.27 mm, the footprint longitudinal axis must be parallel to the transport direction of the PCB. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the PCB. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Typical dwell time is four seconds at 250°C. A mildly−activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual Soldering

Fix the component by first soldering two diagonally−opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.

When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270 and 320°C.

Table 9. Soldering Process

Package	Soldering Method	
	Wave	**Re−flow** (Note 8)
BGA, SQFP	Not suitable	Suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	Not suitable (Note 9)	Suitable
PLCC (Note 10), SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (Notes 10 and 11)	Suitable
SSOP, TSSOP, VSO	Not recommended (Note 12)	Suitable

8. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods.”
9. These packages are not suitable for wave soldering as a solder joint between the PCB and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
10. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
11. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
12. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

Company or Product Inquiries

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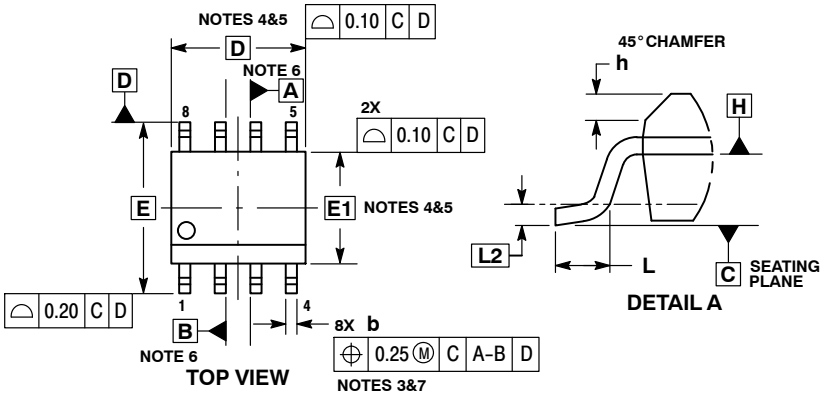
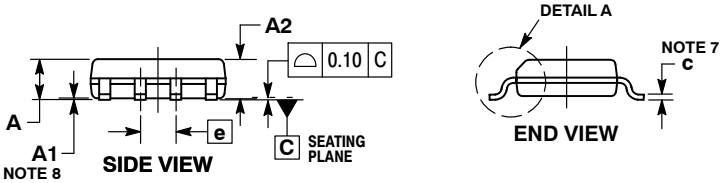
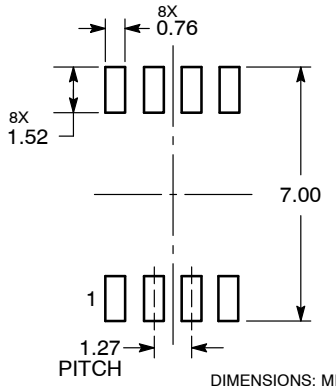




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

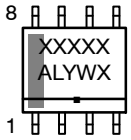
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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