

Quad 2-Input Exclusive-OR Gate

74AC86

General Description

The 74AC86 contains four, 2-input exclusive-OR gates.

Features

- I_{CC} Reduced by 50%
- Outputs Source/Sink 24 mA
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +6.5	V
DC Input Diode Current $V_I = 0.5$ V $V_I = V_{CC} + 0.5$ V	I_{IK}	-20 +20	mA
DC Input Voltage	V_I	-0.5 to $V_{CC} + 0.5$	V
DC Output Diode Current $V_O = -0.5$ V $V_O = V_{CC} + 0.5$ V	I_{OK}	-20 +20	mA
DC Output Voltage	V_O	-0.5 to $V_{CC} + 0.5$	V
DC Output Source or Sink Current	I_O	± 50	mA
DC V_{CC} or Ground Current per Output Pin	I_{CC} or I_{GND}	± 50	mA
Storage Temperature	T_{STG}	-65 to +150	°C
Junction Temperature (PDIP)	T_J	140	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

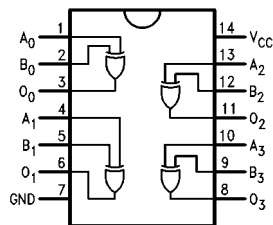


Figure 1. Connection Diagram

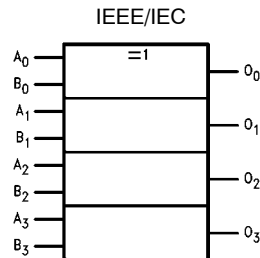
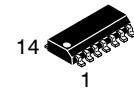
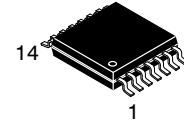


Figure 2. Logic Symbol

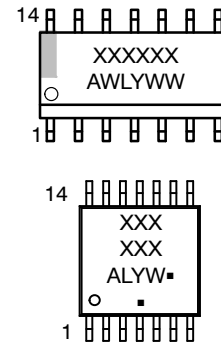


SOIC14
CASE 751EF



TSSOP-14 WB
CASE 948G

MARKING DIAGRAMS



AC86 = Specific Device Code
A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

PIN DESCRIPTION

Pin Names	Description
A ₀ -A ₃	Inputs
B ₀ -B ₃	Inputs
O ₀ -O ₃	Outputs

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	2.0	6.0	V
V_I	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	85	°C
$\Delta V/\Delta t$	Minimum Input Edge Rate V_{IN} from 30% to 70% V_{CC} V_{CC} @ 3.3 V, 4.5 V, 5.5 V	125		mV/ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0	–	2.56	2.46	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = −12 mA I _{OH} = −24 mA I _{OH} = −24 mA (Note 1)
		4.5	–	3.86	3.76		
		5.5	–	4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0	–	0.36	0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA I _{OL} = 24 mA I _{OL} = 24 mA (Note 1)
		4.5	–	0.36	0.44		
		5.5	–	0.36	0.44		
I _{IN} (Note 3)	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OLD}	Minimum Dynamic Output Current (Note 2)	5.5	–	–	75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	–	–	−75	mA	V _{OHD} = 3.85 V Min
I _{CC} (Note 3)	Maximum Quiescent Supply Current	5.5	–	2.0	20.0	μA	V _{IN} = V _{CC} or GND

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0 ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC} .

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 40 pF		Unit
			Min	Typ	Max	Min	Max	
t _{PHL}	Propagation Delay Inputs to Outputs	3.3 5.0	2.0 1.5	6.0 4.5	11.5 8.5	1.5 1.0	12.5 9.5	ns
t _{PLH}	Propagation Delay Inputs to Outputs	3.3 5.0	2.0 1.5	6.5 4.5	11.5 8.5	1.5 1.0	12.5 9.0	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Typ	Unit	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	35	pF	V _{CC} = 5.0 V

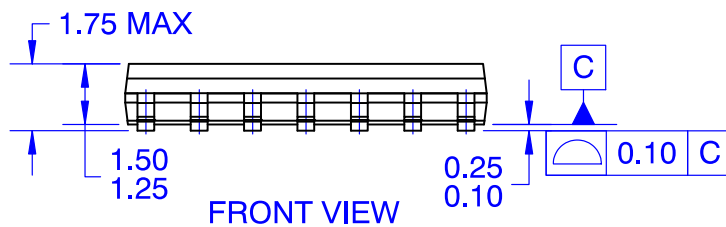
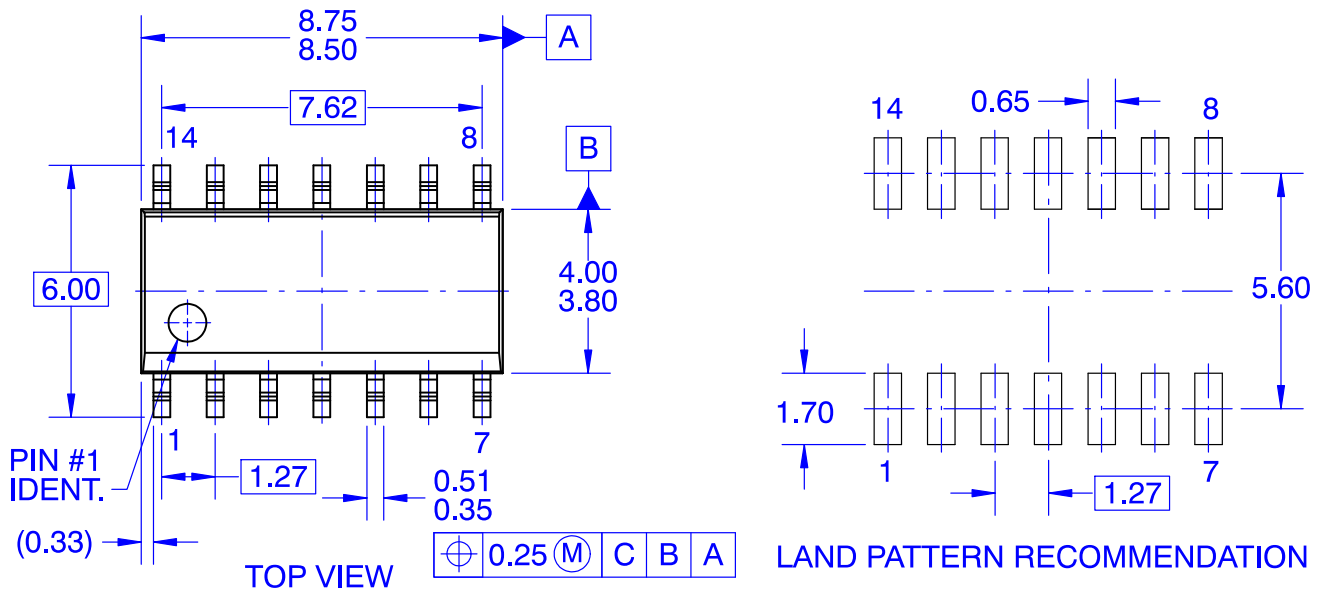
ORDERING INFORMATION

Device	Marking	Package	Shipping†
74AC86MTCX	AC 86	TSSOP-14	2500 Units / Tape & Reel
74AC86SCX	AC86	SOIC-14	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

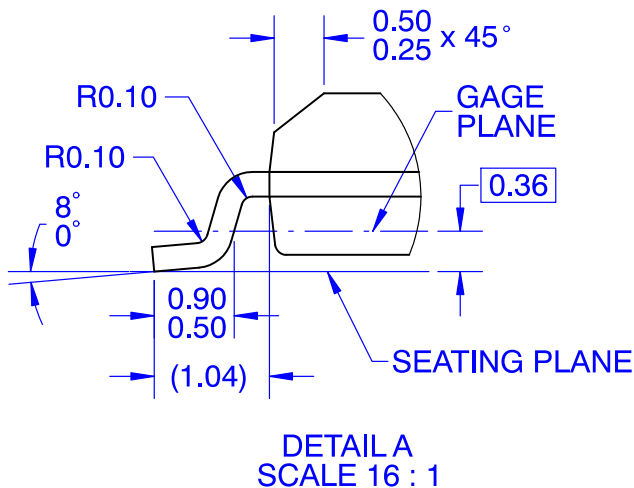
SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



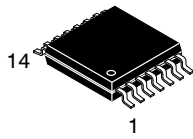
NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009



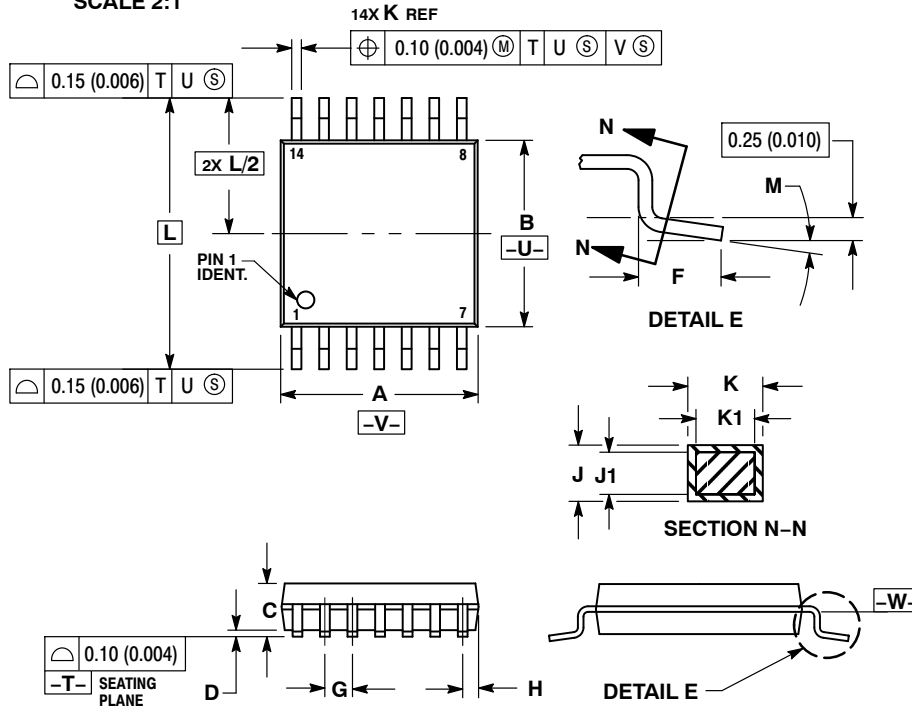
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TSSOP-14 WB
CASE 948G
ISSUE C

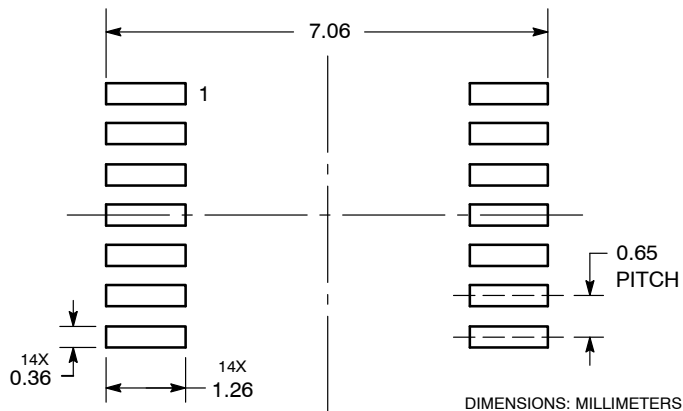
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SCALE 2:1

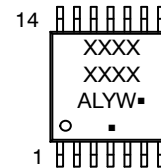

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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